PCT

REQUEST

The undersigned requests that the present international application be processed according to the Patent Cooperation Treaty.

For receiving O[illegible]use only

International Application No.

International Filing Date

Name of receiving Office and "PCT International Application"

Applicant's or agent's file reference 7311 PCT
(if desired) (12 characters maximum)

Box No. I TITLE OF INVENTION
Communication device

Box No. II APPLICANT

Name and address: *(Family name followed by given name; for a legal entity, full official designation The address must include postal code and name of country.)*

Semiconductor Ideas to the Market (ItoM) B.V.

Drielindendreef 53

4389 AH Breda, The Netherlands

☐ This person is also inventor

Telephone No.
+31 76 5309608

Facsimile No.
+31 76 5300496

Teleprinter No.

State *(i.e. country)* of nationality:
NL

State *(i.e. country)* of residence:
NL

This person is applicant for the purposes of: ☐ all designated States ☒ all designated States except the United States of America ☐ the United States of America only ☐ the States indicated in the Supplemental Box

Box No. III FURTHER APPLICANT(S) AND/OR (FURTHER) INVENTOR(S)

Name and address *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country.)*

van Rumpt, Herman Wouter
Neercanne 15
5235 HC s'Hertogenbosch
The Netherlands

This person is:
☐ applicant only
☒ applicant and inventor
☐ inventor only *(If this check-box is marked, do not fill in below.)*

State *(i.e. country)* of nationality:
L

State *(i.e. country)* of residence:
NL

This person is applicant for the purposes of: ☐ all designated States ☐ all designated States except the United States of America ☒ the United States of America only ☐ the States indicated in the Supplemental Box

☐ Further applicants and/or (further) inventors are indicated on a continuation sheet.

Box No. IV AGENT OR COMMON REPRESENTATIVE; OR ADDRESS FOR CORRESPONDENCE

The person identified below is hereby/has been appointed to act on behalf of the applicant(s) before the competent International Authorities as: ☒ agent ☐ common representative

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country.)*

Joop van Straaten
Octrooibureau van Straaten B.V.
Waalreseweg 17

Telephone No.
+31 40 208 9226

Facsimile No.
+31 40 204 3915

Box No.V DESIGNATION OF STATES

The following designations are hereby made under Rule 4.9(a) *(mark the applicable check-boxes; at least one must be marked):*

Regional Patent

- [ ] **AP** **ARIPO Patent:** KE Kenya, LS Lesotho, MW Malawi, SD Sudan, SZ Swaziland, UG Uganda and any other State which is a Contracting State of the Harare Protocol and of the PCT
- [ ] **EA** **Eurasian Patent:** AZ Azerbaijan, BY Belarus, KZ Kazakstan, RU Russian Federation, TJ Tajikistan, TM Turkmenistan, and any other State which is a Contracting State of the Eurasian Patent Convention and of the PCT
- [X] **EP** **European Patent:** AT Austria, BE Belgium, CH and LI Switzerland and Liechtenstein, DE Germany, DK Denmark, ES Spain, FR France, GB United Kingdom, GR Greece, IE Ireland, IT Italy, LU Luxembourg, MC Monaco, NL Netherlands, PT Portugal, SE Sweden, and any other State which is a Contracting State of the European Patent Convention and of the PCT
- [ ] **OA** **OAPI Patent:** BF Burkina Faso, BJ Benin, CF Central African Republic, CG Congo, CI Côte d'Ivoire, CM Cameroon, GA Gabon, GN Guinea, ML Mali, MR Mauritania, NE Niger, SN Senegal, TD Chad, TG Togo, and any other State which is a member State of OAPI and a Contracting State of the PCT *(if other kind of protection or treatment desired, specify on dotted line)*..............................

National Patent *(if other kind of protection or treatment desired, specify on dotted line):*

- [ ] **AM** Armenia
- [ ] **AT** Austria
- [ ] **AU** Australia
- [ ] **BB** Barbados
- [ ] **BG** Bulgaria
- [ ] **BR** Brazil
- [ ] **BY** Belarus
- [ ] **CA** Canada
- [ ] **CH and LI** Switzerland and Liechtenstein
- [ ] **CN** China
- [ ] **CZ** Czech Republic
- [ ] **DE** Germany
- [ ] **DK** Denmark
- [ ] **EE** Estonia
- [ ] **ES** Spain
- [ ] **FI** Finland
- [ ] **GB** United Kingdom
- [ ] **GE** Georgia
- [ ] **HU** Hungary
- [ ] **IS** Iceland
- [X] **JP** Japan
- [ ] **KE** Kenya
- [ ] **KG** Kyrgyzstan
- [ ] **KP** Democratic People's Republic of Korea
- [ ] **KR** Republic of Korea
- [ ] **KZ** Kazakhstan
- [ ] **LK** Sri Lanka
- [ ] **LR** Liberia
- [ ] **LT** Lithuania
- [ ] **LU** Luxembourg
- [ ] **LV** Latvia
- [ ] **MD** Republic of Moldova
- [ ] **MG** Madagascar
- [ ] **MN** Mongolia
- [ ] **MW** Malawi
- [ ] **MX** Mexico
- [ ] **NO** Norway
- [ ] **NZ** New Zealand
- [ ] **PL** Poland
- [ ] **PT** Portugal
- [ ] **RO** Romania
- [ ] **RU** Russian Federation
- [ ] **SD** Sudan
- [ ] **SE** Sweden
- [ ] **SG** Singapore
- [ ] **SI** Slovenia
- [ ] **SK** Slovakia
- [ ] **TJ** Tajikistan
- [ ] **TM** Turkmenistan
- [ ] **TT** Trinidad and Tobago
- [ ] **UA** Ukraine
- [ ] **UG** Uganda
- [X] **US** United States of America
- [ ] **UZ** Uzbekistan
- [ ] **VN** Viet Nam

Check-boxes reserved for designating States (for the purposes of a national patent) which have become party to the PCT after issuance of this sheet:

- [ ] ....
- [ ] ....
- [ ] ....
- [ ] ....

In addition to the designations made above, the applicant also makes under Rule 4.9(b) all designations which would be permitted under the PCT except the designation(s) of ______________________________

The applicant declares that those additional designations are subject to confirmation and that any designation which is not confirmed

Box No. VI PRIORITY CLAIM Further priority claims are indicated in the Supplemental Box ☐

The priority of the following earlier application(s) is hereby claimed:

	Country *(in which, or for which, the application was filed)*	Filing Date *(day/month/year)*	Application No.	Office of filing *(only for regional or international application)*
item (1)	EP	19/04/1999 (19 April 1999)	99201195.7	EPO
item (2)				
item (3)				

Mark the following check-box if the certified copy of the earlier application is to be issued by the Office which for the purposes of the present international application is the receiving Office (a fee may be required):

[x] The receiving Office is hereby requested to prepare and transmit to the International Bureau a certified copy of the earlier application(s) identified above as item(s) :

Box No. VII INTERNATIONAL SEARCHING AUTHORITY

Choice of International Searching Authority (ISA) *(If two or more International Searching Authorities are competent to carry out the international search, indicate the Authority chosen; the two-letter code may be used):* ISA /

Earlier search *Fill in where a search (international, international-type or other) by the International Searching Authority has already been carried out or requested and the Authority is now requested to base the international search to the extent possible, on the results of that earlier search. Identify such search or request either by reference to the relevant application (or the translation thereof) or by reference to the search request*

Country (or regional Office): Date *(day/month/year)*: Number:

Box No. VIII CHECK LIST

This international application contains the following number of sheets:

1. request	:3	sheets
2. description	:15	sheets
3. claims	:5	sheets
4. abstract	:1	sheets
5. drawings	:6	sheets
Total	:30	sheets

This international application is accompanied by the item(s) marked below:

1. [ ] separate signed power of attorney
2. [x] copy of general power of attorney
3. [ ] statement explaining lack of signature
4. [ ] priority document(s) *identified in Box No VI as item(s):*
5. [x] fee calculation sheet
6. [ ] separate indications concerning deposited microorganisms
7. [ ] nucleotide and/or amino acid sequence listing (diskette)
8. [ ] other *(specify)*:

Figure No. 1 of the drawings (if any) should accompany the abstract when it is published.

Box No. IX SIGNATURE OF APPLICANT OR AGENT

Next to each signature, indicate the name of the person signing and the capacity in which the person signs (if such capacity is not obvious from reading the request)

Joop v Straaten, agent

For receiving Office use only

1. Date of actual receipt of the purported international application:
2. Drawings: [ ] received [ ] not received
3. Corrected date of actual receipt due to later but timely received papers or drawings completing the purported international application:
4. Date of timely receipt of the required corrections under PCT Article 11(2):
5. International Searching Authority specified by the applicant: ISA/
6. [ ] Transmittal of search copy delayed until search fee is paid

For International Bureau use only

Date of receipt of the record copy by the International Bureau:

This sheet is no   t of and does not count as a sheet of the internat   application.

PCT

FEE CALCULATION SHEET

Annex to the Request

For receiving Office use only
International application No.
Date stamp of the receiving Office

Applicant's or agent's file reference 7311 PCT

Applicant
Semiconductor Ideas to the Market (ItoM) B.V.

CALCULATION OF PRESCRIBED FEES

1. TRANSMITTAL FEE .... 102 [T]

2. SEARCH FEE .... 945 [S]
   International search to be carried out by ______
   (If two or more International Searching Authorities are competent in relation to the international application, indicate the name of the Authority which is chosen to carry out the international search.)

3. INTERNATIONAL FEE

   Basic Fee
   The international application contains 30 sheets.
   first 30 sheets .... 409 [b_1]
   ______ x ______ = ______ [b_2]
   remaining sheets   additional amount

   Add amounts entered at b_1 and b_2 and enter total at B .... 409 [B]

   Designation Fees
   The international application contains 3 designations
   3 x 88 = 264 [D]
   number of designation fees payable *(maximum 11)*   amount of designation fee

   Add amounts entered at B and D and enter total at I .... 673 [I]
   (Applicants from certain States are entitled to a reduction of 75% of the international fee. Where the applicant is (or all applicants are) so entitled, the total to be entered at I is 25% of the sum of the amounts entered at B and D.)

4. FEE FOR PRIORITY DOCUMENT .... 45 [P]

5. TOTAL FEES PAYABLE
   Add amounts entered at T, S, I and P, and enter total in the TOTAL box 1765
   TOTAL

☐ The designation fee is not paid at this time.

MODE OF PAYMENT

☐ authorization to charge deposit account (see below)	☒ bank draft	☐ coupons
☐ cheque	☐ cash	☐ other *(specify)*:
☐ postal money order	☐ revenue stamps	

DEPOSIT ACCOUNT AUTHORIZATION *(this mode of payment may not be available at all receiving Offices)*

The RO/ ______

☐ is hereby authorized to charge the total fees indicated above to my deposit account.

☐ is hereby authorized to charge any deficiency or credit any overpayment in the total fees indicated above to my deposit account.

☐ [illegible]

1 **ALLGEME[illegible]E VOLLMACHT**
GENERAL AUTHORISATION
POUVOIR GENERAL

Nur [illegible]ichen Gebrauch / For of[illegible]al use only / Cadr[illegible]ervé à l'administration
Nr. der allgemeinen Vollmacht / General Authorisation No. / N° du pouvoir général

2 Ich (Wir) / I (We) / Je (Nous)

Semiconductor Ideas to the Market (ItoM) B.V.
Drielindendreef 53
4389 AH Breda
The Netherlands

3 bevollmächtige(n) hiermit / do hereby authorise / autorise (autorisons) par la présente

Joop van Straaten
Octrooibureau van Straaten B.V.
Waalreseweg 17
5554 HA Valkenswaard
The Netherlands

4 mich (uns) in den durch das Europäische Patentübereinkommen und den Vertrag über die internationale Zusammenarbeit auf dem Gebiet des Patentwesens geschaffenen Verfahren in allen meinen (unseren) Patentangelegenheiten zu vertreten, alle Handlungen für mich (uns) vorzunehmen und Zahlungen für mich (uns) in Empfang zu nehmen. Untervollmacht kann erteilt werden.

to represent me (us) in all proceedings established by the European Patent Convention and by the Patent Cooperation Treaty and to act for me (us) in all patent transactions and to receive payments on my (our) behalf. Sub-authorisation may be given.

à me (nous) représenter pour ce qui concerne toutes mes (nos) affaires de brevet dans toute procédure instituée par la Convention sur le brevet européen et par le Traité de coopération en matière de brevets et, à ce titre, à agir en mon (notre) nom et à recevoir des paiements pour mon (notre) compte. Le pouvoir pourra être délégué.

☐ Weitere Vertreter sind auf einem gesonderten Blatt angegeben. / Additional representatives indicated on supplementary sheet. Les autres mandataires sont mentionnés sur une feuille supplémentaire.

5 ☒ Bitte die gelbe Kopie, ergänzt um die Nr. der allgemeinen Vollmacht, an den Vollmachtgeber zurücksenden.
Please return the yellow copy, supplemented by the General Authorisation No., to the authorisor.
Prière de renvoyer la copie jaune au mandant, munie du n° du pouvoir général.

Ort/Place/Lieu
Breda

Datum/ Date
25/02/2000

Unterschrift(en) / Signature(s)

6 Petrus Johannes Karel Langendam, Managing Director

Das Formblatt muß vom (von den) Vollmachtgeber(n) (bei juristischen Personen vom Unterschriftsberechtigten) eigenhändig unterzeichnet sein. Nach der Unterschrift bitte den (die) Namen des (der) Unterzeichneten mit Schreibmaschine wiederholen (bei juristischen Personen die Stellung des Unterschriftsberechtigten innerhalb der Gesellschaft angeben).

The form must bear the personal signature(s) of the authorisor(s). (In the case of legal persons, that of the officer empowered to sign) After the signature, please type the name(s) of the signatory(ies) adding, in the case of legal persons, his (their) position within the company.

Le formulaire doit être signé de la propre main du (des) mandant(s) (dans le cas de personnes morales, de la pers[illegible]

PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 5 : H03F 3/217	A1	(11) International Publication Number: WO 92/14300 (43) International Publication Date: 20 August 1992 (20.08.92)

(21) International Application Number: PCT/US92/00844

(22) International Filing Date: 30 January 1992 (30.01.92)

(30) Priority data:
650,789 4 February 1991 (04.02.91) US

(60) Parent Application or Grant
(63) Related by Continuation
US 650,789 (CIP)
Filed on 4 February 1991 (04.02.91)

(71) Applicant *(for all designated States except US)*: ADVANCED ENERGY INDUSTRIES, INC. [US/US]; 1600 Prospect Parkway, Fort Collins, CO 80525 (US).

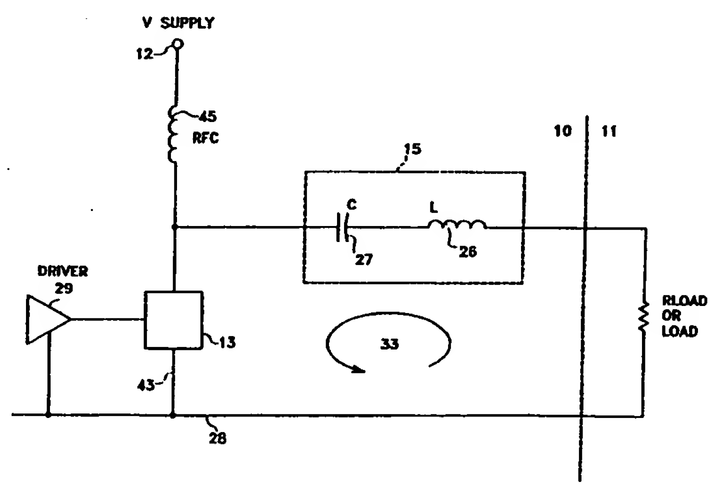
(72) Inventors; and
(75) Inventors/Applicants *(for US only)* : PORTER, Robert, M., Jr. [US/US]; 1501 Redberry Court, Fort Collins, CO 80525 (US). MUELLER, Michael, L. [US/US]; 1629 East 16th Street, Loveland, CO 80537 (US).

(74) Agent: SANTANGELO, Luke, R.; 315 W. Oak Street, Suite 701, Fort Collins, CO 80521 (US).

(81) Designated States: AT (European patent), BE (European patent), CH (European patent), DE (European patent), DK (European patent), ES (European patent), FR (European patent), GB (European patent), GR (European patent), IT (European patent), JP, LU (European patent), MC (European patent), NL (European patent), SE (European patent), US.

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: HIGH POWER SWITCH-MODE RADIO FREQUENCY AMPLIFIER METHOD AND APPARATUS



(57) Abstract

Disclosed are both methods and a circuit to achieve powers of many kilowatts in radio frequency amplification using a switch mode amplifier in a new class of operation. In operation the invention utilizes internal switch characteristics. Methods create a substantial voltage step at the end of a response time period which allows greater output power without increasing the maximum switch voltage, reduces the maximum switch voltage for the same power, and which permits reduction of the stress on the switch element. Utilization of internal varactor capacitance avoids undesirable circulating currents and avoids the effects of lead inductance. The design allows use of less expensive components and high voltage switches not manufactured for radio frequency applications by preferring a substantial internal capacitance to establish maximum power. Other components of the network circuitry are also coordinated with the internal varactor capacitance. Adjustment of the conduction angle for optimum power and elimination of a need to bias the driver are also disclosed.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria
AU	Australia
BB	Barbados
BE	Belgium
BF	Burkina Faso
BG	Bulgaria
BJ	Benin
BR	Brazil
CA	Canada
CF	Central African Republic
CG	Congo
CH	Switzerland
CI	Côte d'Ivoire
CM	Cameroon
CS	Czechoslovakia
DE	Germany
DK	Denmark
ES	Spain
FI	Finland
FR	France
GA	Gabon
GB	United Kingdom
GN	Guinea
GR	Greece
HU	Hungary
IE	Ireland
IT	Italy
JP	Japan
KP	Democratic People's Republic of Korea
KR	Republic of Korea
LI	Liechtenstein
LK	Sri Lanka
LU	Luxembourg
MC	Monaco
MG	Madagascar
ML	Mali
MN	Mongolia
MR	Mauritania
MW	Malawi
NL	Netherlands
NO	Norway
PL	Poland
RO	Romania
RU	Russian Federation
SD	Sudan
SE	Sweden
SN	Senegal
SU	Soviet Union
TD	Chad
TG	Togo
US	United States of America

HIGH POWER SWITCH-MODE RADIO FREQUENCY AMPLIFIER METHOD AND APPARATUS

I. TECHNICAL FIELD

The present invention relates generally to the field of radio frequency (RF) power amplifiers, focusing on the aspects involved in the field when RF power amplifiers are utilized to generate high power outputs. More particularly the invention pertains to the narrow field of high power RF amplifiers having switching devices and configured similarly to those operating in a Class E mode.

II. BACKGROUND OF THE INVENTION

Radio frequency circuit design, unlike circuit design at the lower frequencies, is a field which involves an interplay between the theoretical and the practical. While it is characterized by the same fundamental theoretical relationships well known to almost any circuit designer, across the range of frequencies involved, practical effects also become important. As a result, circuit designers in this field are often required to simultaneously understand and apply the theory of operation of each device, the function of each device as it actually operates, and the ability to experimentally attempt and reconcile results achieved. In actually fashioning circuits and devices to achieve extreme levels of performance, this latter aspect —— the ability to experimentally attempt and reconcile results achieved —— becomes very significant as achievements seemingly straightforward from a theoretical basis become increasingly difficult to realize. In this regard, one of the challenges faced is that of understanding and utilizing the theoretical preconceptions while remaining open minded enough to go beyond the limits described by them.

The relevant field is also unique in that seemingly insignificant changes in existing circuitry can entirely change the operation of the device. As a result of this fundamental aspect, those skilled in the art have developed a shorthand technique by which several combinations of operating parameters and resultant conditions may be characterized and utilized. This shorthand technique is that of

describing amplifiers in terms of classes of operation. To the RF circuit designer, in many cases, amplification circuits which are almost identically arranged and yet function very differently can be discerned by the simple characterization of the amplifier's "class" of operation. In application, these "classes" (referred to as Class A, Class B, etc.) have become an important tool to the RF amplifier designer. For example, by merely stating that an amplifier operates in the Class E mode, those skilled in the art are able to apply such a amplifier often without the need to fully calculate theoretically the effects of that amplifier in advance of its actual application. This design technique has obviously advantages. It does, however create limitations. As it applies to the present invention, one of these limitations is that it fosters the acceptance of some preconceptions and assumed restrictions which are now proven to be unnecessary and even erroneous.

In creating RF power amplifiers, some of the goals those skilled in the art have long sought are those of higher power (powers above a few hundred watts for a single stage device), higher efficiency, and greater simplicity to lessen the cost, components, and space required for the amplifier. Each of these challenges have been addressed by those skilled in the art to varying degrees. With respect to some of these a significant advance —— and a new class of operation —— was invented in 1975 through US patent 3919656. This invention, now referred to as a "Class E" amplifier, typified invention in this field. Although that amplifier was configured almost identically to its prior art, through a new selection of parameters, its operation acted differently to achieve significantly improved results. This is also true of the present invention.

As an incident of the new class of operation, however, the teachings of the Class E amplifier also resulted in a new set of preconceptions and assumed restrictions. While many of these preconceptions and restrictions made sense at the time of the original Class E invention, they continued even after their original reason for being ceased. These included an almost dogmatically pursued desire for efficiency, a theoretical design model that ignored significant internal component characteristics, and an assumed restriction on the maximum amount of power possible. In overcoming each of these facets, the present invention achieves

perhaps dramatic performance advantages. With respect to the aspect of maximum power, the present invention affords a dramatic improvement. Where the prior art devices were capable of claiming the ability to consistently produce power in the range of two hundred watts and in isolated instances produce 1000 watts, without yet having identified its upper limits, the present invention can easily produce many times this amount. Where the prior art devices required the use of expensive RF switching devices in order to achieve their levels of performance, the present invention requires only inexpensive switches to achieve similar performance levels. Where the prior art devices rigidly adhered to achieving efficiency through the constraint of pursuing zero voltage at the instant of switch turn-on, the present invention departs sharply to teach a substantial voltage at such time. Perhaps most importantly, however, the present invention discloses a more accurate method of designing high power RF amplifier circuitry whereby a broad variety of improvements in performance can be achieved and whereby each of these improvements may be optimized for different applications.

Certainly other developments have attempted to improve the original Class E amplifier. In 1984, US patent number 4449174 recognized in a somewhat different field that the internal capacitance of the switch was significant for some circuits. In contrast to the present invention, however, it applied this aspect in a manner which reinforced the preconception that efficiency is paramount and can only be maintained through the zero voltage constraint at the instant of switch turn-on. That those skilled in the relevant art continued in this preconception is clear. In the 1987 RF Design article by one of the well-respected original Class E inventors entitled "Power Transistor Output Port Model," those skilled in the art were told not to stray from the zero voltage condition. In 1988 US patent number 4743858, in proposing the use of a diode for better device utilization for the Class E amplifier, again reiterated the desire to avoid voltage at the instant of switch turn-on.

The seemingly simple recognition that internal aspects of the switch were important did not alone lead to the present invention. After the 1984 patents lead, the 1985 Motorola RF Device Data article entitled "Applying Power MOSFETs in

Class D/E RF Power Amplifier Design" by Helge Granburg not only presented the power level limits thought to be practically achievable (power level limits many times less than those possible through the present invention), but it also lead those skilled in the art to ignore important effects of lead inductance which were to have significant impacts on the design of the present invention. In addition, in the 1990 US patent number 4891746 in a field similar to the 1984 US patent number 4449174, the continued adherence to efficiency even taught those skilled in the art away from the important aspect of a voltage step. Although arguably in a different field, this art may have lead those skilled in the present field away from the aspect of maintaining a positive voltage across the switch which also becomes paramount at the higher power levels.

As can be seen, each of these prior efforts actually taught away from directions taken by the present invention and served to reinforce attitudes which in essence limited prior designs. This was true even though there was a well-known and long-felt need to achieve the performance of the present invention were well known and had existed. While those skilled in the art appreciated the goals of the present invention, their attempts to achieve such goals were inadequate because they failed to recognize the effect of their preconceptions. Even the unexpectedly simple and seemingly minor modifications presented by the present invention appears to have lead those skilled in the art to assume the direction taken by it would not yield the sometimes dramatic improvements achieved by it. This may also have been reinforced by the prior feeling that since an incremental increase in performance was difficult, a significant leap in performance was also difficult. By breaking from traditions long adhered to in the relevant art, the present invention proves this completely incorrect.

III. DISCLOSURE OF INVENTION

The present invention discloses a technique and device to amplify and generate a high power radio frequency signal. Rather than affording an incremental increase in performance over the prior art, the invention utilizes techniques and circuitry which were previously considered undesirable to achieve significant leaps

in performance and other criteria compared to the prior art. It also allows for different modes of operation whereby goals such as power, size, cost, and reliability can be optimized depending upon the particular application.

In general terms, the invention involves both methods and embodiments of an apparatus. Each of these achieve several different objects which, when combined, act to achieve the mentioned leaps in performance. In one embodiment, the invention discloses a switch-mode RF amplifier which creates a substantial voltage step at the end of the non-conductive time period to achieve different results ranging from allowing more RF power to be generated to allowing a less expensive switch to be used. In another embodiment, undesirable internal switch characteristics are actually utilized in a uniquely desirable way to minimize problematic RF effects at the higher frequencies and powers such as in the HF range. In another embodiment, the undesirable internal switch characteristics are used to lessen sensitivity of the amplifier to tuning. In yet another embodiment, designs are used which simplify and lessen the space, and increase the power densities, required for RF amplifiers.

Importantly, the invention breaks from several time-honored traditions in RF power amplification. While drawing from some of the operating conditions used in Class E operation, the invention expands upon these conditions in a manner which could be characterized as a new, unique class of operation. With simpler circuitry, the invention teaches the selection and coordination of network components to allow a voltage step in the response waveform and to eliminate a current loop previously utilized. By recognizing and utilizing (rather than avoiding or compensating for) the inherent characteristics in realistic switches, the invention achieves its goals.

Accordingly, a general object of the present invention is to provide techniques and devices which achieve performance with respect to a variety of criteria. In keeping with this broad goal, it is an object of the invention to allow optimization to each application as desired.

One object of the present invention is to provide an RF power amplifier which can achieve power levels beyond the limits of those experienced by the prior art devices. In achieving the leap in power levels, an object is to maintain reliability standards consistent with or above those existing for the prior art. The invention also is designed to avoid the creation of unusual limitations peculiar to the design and allows operation with frequency sensitivities consistent with the prior art devices.

It is also a general object of the present invention to provide designs and techniques which afford manufacturing and commercial advantages. Another object of the present invention is to reduce the complexity and number of components required in the amplification circuitry. In achieving this goal, the invention has several different goals and objects. Practically, it is an object to allow a design which is less expensive to manufacture. This is achieved both through the use of fewer components and the use of even less expensive individual components. For some applications, it is an object to provide a design which is smaller. Naturally this may enhance the scope of application of such amplifiers.

Another object of the present invention is to overcome the limitations encountered in some operating parameters. At higher frequency and power, the effects of circulating currents have previously posed limitations. The present invention overcomes these limitations and as a result allows performance leaps. An object in this regard is to minimize circulating currents and improve output form.

Yet another object of the present invention is to accommodate existing switch designs and limitations. In achieving this object, the invention not only avoids the need to overcome switch limitations, but actually utilizes the inherent characteristics of a practical transistor switch to achieve its performance abilities. One of the modes in which the present invention can be configured acts to address the voltage breakdown limitations found for many switches. In so doing it has as an object the reduction of the voltage to which the switch is subjected. The invention also allows designers to recognize the impact of the inherent

characteristics of practical switches. An object of the invention is to disclose to designers the relationship between switch characteristics and circuit performance. Once the character of the switch is determined, the designer may coordinate all of the circuit's other components to optimize a variety of operating parameters.

It is also an object of the invention to allow for ways in which power may be maximized without changing components of the circuitry. Recognizing that not all performance parameters can be accurately predicted by current theoretical understandings, an object is to allow practical implementation in different applications and embodiments.

A further object of the invention is to provide techniques and designs whereby trade-offs may be accepted by the designer to optimize specific performance parameters depending upon application. In this regard, an object is to utilize some trade-offs, one example being that of efficiency, in a manner that allows offsetting gains such that the result in only minor changes and yet still realizes the performance advances desired.

Naturally, further objects of the invention are disclosed throughout other areas of the specification and claims.

IV. BRIEF DESCRIPTION OF DRAWINGS

Figure 1 is a circuit diagram of an embodiment of the invention.

Figures 2a and 2b are representations of the voltage and current waveforms during the response and conductive time periods, respectively.

Figures 3a and 3b are representations of the voltage and current waveforms of prior art devices during the response and conductive time periods, respectively.

Figure 4 is a schematic representation of a realistic FET switch device.

Figure 5 is a circuit diagram of the typical prior art device showing the current loops which exist.

V. BEST MODE(S) FOR CARRYING OUT THE INVENTION

As can be seen from the drawings, and in keeping with an object of the invention, the basic concepts of the present invention are easily implemented. Figure 1 shows the present invention as it is currently configured. In understanding the degree to which this new circuit and the potentially new class of operation can be varied, it should be understood that at present, the performance boundaries have not yet been established. Accordingly, it is anticipated that refinements to the present understanding may continue to be added and additional performance achieved. By virtue of the fact that the present invention embarks in a completely new direction, it should be understood that such refinements and improvements will fall within the scope of the present invention and its claims.

Referring to Figure 1, it can be seen that the invention is most simply characterized as a single loop RF power amplifier in which power amplifier (10) is combined with load (11) to create network current loop (33). Although shown schematically as a resistor, it should be understood that load (11) may be any device which utilizes power and may have its own reactive aspects as well. In addition, it should be understood that this power may be supplied either in a continuous, pulsed, or even amplitude modulated manner. External to network current loop (33) are the well-known elements (shown in schematic) of voltage supply (12) and radio frequency driver (29). As is also well-known to those skilled in the art, voltage supply (12) includes RF choke (45). Network current loop (33) includes reactive network circuitry (15) including, in simplified form, serially-connected inductor (26) and separate capacitor (27). These are also serially connected to switch (13). Switch (13) and load (11) are connected to common voltage reference (28) to complete network current loop (33). In this manner, switch has common lead (43) well defined.

Although the amplifier can be arranged to look very similar to a Class E amplifier, it functions differently in many regards. [Much like the original Class E amplifier does with respect to its predecessors.] Like a Class E amplifier the present invention has inherently high efficiency and is relatively simple. Class E amplifiers in general, however, are designed such that when the switch transitions from "off" (its non-conductive state) to "on" (its conductive state) the voltage across it is essentially zero during the switching transition. This is in sharp contrast to the present invention. While in Class E operation, this condition is desired to minimize turn-on or step losses, an exactly opposite condition —— that of a substantial voltage step —— is desired by the present invention to achieve performance improvements. In Class E operation, the network causes the waveform across the transistor to approach both a zero voltage and a zero slope at the end of the "off" state. The present invention does not require these restrictions. As a result, all aspects of the circuit may be optimized for high output power. The result is a single stage RF amplifier which may operate efficiently at power levels of many kilowatts.

This new class of operation and its differences from the prior art may be further understood with reference to figures 2, 3, and 4. Referring to figure 2, it can be seen that both voltage and current waveforms for switch (13) are shown during its conductive and non-conductive states. Starting with conductive time period (30), it can be seen that at turn-on time (22), current begins to flow through switch element (14) of switch (13) in a manner which creates current waveform (44). Current waveform (44) is thus conditioned by network current loop (33) as well as voltage supply (12) and radio frequency driver (29). As is well-known, current waveform results from the energy provided by voltage supply (12) while switch is in its conducting state. This energy is to some extent stored in inductor (26) and separate capacitor (27) to cause response voltage waveform (46). As is explained later, current waveform (44) in this class of operation includes current spike (39) in all cycles after the initial cycle which is not shown. Current waveform (44) is abruptly driven to zero at the end of conduction time period (30) by the transition of switch (13) to its non-conducting state at turn-off time (23). This transition is accomplished rapidly such that no significant active region exists

in the switch transition. Some slope is shown, however, since practical devices do require some time to transition. This type of rapid transition, commonly referred to as the switching mode of operation or switch-mode, the operation of switch (13) is utilized very differently than when the active region (the regime in which the switch acts only partially open) causes the desired effect. In making the transition between states, it should be understood that by driving switch (13) through the use of greater than necessary voltages, less expensive, slow acting switch devices may be used.

Immediately after the transition of switch (13) to its non-conducting state, the energy stored in inductor (26), separate capacitor (27), and otherwise within network current loop (33) acts to create response voltage waveform (46) across switch (13), specifically across varactor capacitor (38), for response time period (31). Response voltage waveform (46) is thus conditioned by the components in network current loop (33) and as shown is time-varying as desired to obtain the appropriate output result. During this time, response voltage waveform (46) reaches a maximum response voltage (47) which is relative to supply voltage (25). As mentioned earlier, in this class of operation, response voltage waveform (46) is such that at the end of response time period (31) or the time immediately prior to turn-on time (22), a substantial voltage step (24) remains. When switch (13) is next caused to transition to its conducting state, the energy caused by voltage step (24) acts to cause previously mentioned current spike (39).

Comparing this sequence of events with those shown in figure 3 for a Class E RF amplifier, the differences between this class of operation and the Class E mode of operation can be readily understood. As can be seen in figure 3, there exists both Class E current waveform (16) and Class E voltage waveform (17). Importantly, in Class E operation, the choice of circuit elements and conduction angle forces the voltage to be zero at a time immediately prior to turn-on time (22). As a result, no current spike exists in Class E operation. This avoids assumed "significant" power losses associated with such a current spike, as previously desired by those skilled in the art as such avoidance was presumed to allow for improvements in efficiency. As can be seen in figure 3, the shape of

Class E voltage waveform (17) initially rises and finally falls more rapidly than that shown in figure 2. In addition, the height of current waveform (44), not including that of current spike (39), will also be lower than that of corresponding Class E current waveform (16) for the same maximum response voltage (47).

In regard to the operation of the present invention there are several things to note. First, there is indeed some loss in the switching device due to current spike (39). The amount of this loss is dependent upon internal conditions which realistically exist in practical switches, namely, the internal capacitance of switch (13). Second, current spike (39) does subject switch (13) briefly to more extreme conditions than that of a Class E amplifier. This is also dependent upon internal conditions which realistically exist in practical switches and is an effect which can practically be accommodated. As may begin to be understood, the present invention was required to incorporate not just a theoretical model of the amplifier's operation, but it was also required to incorporate practical considerations of devices as they actually exist. In this way it was able to achieve its performance improvements over the prior art.

Achieving high power from a single switch RF amplifier is theoretically straightforward when utilizing an ideal switch. In order to approximate the results achieved while using practical switches, however, internal capacitance (including voltage-variable, or varactor capacitance), lead inductance, voltage limitations, and "on" resistance must be added to the switch model. In cases where the switch utilized is a field effect transistor (FET), the internal reverse diode must also be considered. In trying to obtain power levels of many kilowatts from a circuit using a single switch, many of the non-ideal characteristics of the switch must be known and accounted for in the circuitry and operation of the switch-mode radio frequency (RF) amplifier. Some of the limiting factors for obtaining high power levels at high frequencies have not yet been identified in many Class E RF amplifiers. New concepts are required to obtain these higher output powers.

A practical transistor switch (as currently designed), whether a bipolar device or an FET, has numerous particular electrical characteristics, several of

which are important to the present invention. Referring to Figure 4, a schematic representation of a realistic FET switch device, three of these characteristics can be seen. First, such a switch includes several capacitance elements. The most important of these is shown in Figure 4 as varactor capacitor (38) which exists parallel to switch element (14). Second, parallel to varactor capacitor (38) within a FET switch there exists reverse diode (41). Importantly to some aspects of the present invention, and as described later, it should be understood that reverse diode (41) is such that it can be subject to failure if rapidly transitioned from negative to positive voltage. Third, and also important to other aspects of the present invention, the common and output (non-drive) connections of switch (13) include lead inductances (32). These are uniquely accommodated by the present invention and play an important part in developing the initial theoretical understanding of the function of the present invention. With respect to this understanding, it should be understood that many aspects of the invention may vary as switch and other component design evolves. In this regard, it should be understood that such variations will fall within the scope of the present invention, its essence lying more fundamentally with the design realizations and discoveries achieved than merely the particular circuit designs developed.

With respect to varactor capacitor (38), it should be understood that this type of internal capacitance varies as a function of the output voltage. The internal output varactor capacitance changes inversely proportional to the square root of the voltage across it for any significant voltage. Since in many single switch RF amplifiers this capacitance is a significant component in the circuit, the resulting output voltage waveform is significantly affected.

In prior art Class E amplifiers, the theoretical ratio of the peak voltage across the switch to the supply voltage for optimum Class E operation is approximately 3.56:1, assuming constant output capacitance. This is only true for a switching device whose output capacitance is fixed with respect to the voltage across it; it is not true when varactor capacitor (38) is in fact present. In such a case, this ratio is actually higher, thus such devices would (prior to the present invention) have dictated lower power outputs. In regards to the present invention this aspect

alone may have lead those skilled in the art to assume that in order to supply similar power levels and loads, a switch having an internal varactor capacitor (38) would require maximum response voltage (47) more than 25% higher than that for a constant output capacitance. Therefore, for a maximum allowable peak voltage across a switch utilizing only the varactor capacitance, prior theory would have lead those skilled in the art to believe that it was not possible to achieve the theoretical output power of a Class E amplifier.

In sharp contrast to such predictions, the use of varactor capacitor (41) as the only capacitive circuit element which is parallel to the switch actually provides the advantage of reducing the slope of the response voltage curve at turn-off of the switch. This reduces the power dissipated in the switch during its turn-off transient, as the instantaneous product of the voltage across it and the current through it during the turn-off period is reduced by the reduction of the slope.

Naturally, the effect of varactor capacitor (38) on response voltage waveform (46) can be lessened by providing an external fixed capacitor across the output of the transistor as shown in the original Class E patent. As a result, for the same loading and output power, the voltage across the switch will not be as great as it would with varactor capacitor (38) alone. Referring to figure 5, a disadvantage of paralleling an external fixed capacitor in an attempt to obtain multikilowatt power levels at high frequencies can be seen. This is due to the effect of switch current loop (34) which the parallel capacitor creates. It can be seen that when such a configuration is pursued, an additional loop, switch current loop (34), is created defined by the switch's varactor capacitor (38), its lead inductances (32), and the external capacitor (42). Thus in prior art devices utilizing external capacitor (42) the designer need not only contend with the effects of a single network current loop (33), but rather with its equivalent, the prior art main network current loop (48), switch current loop (34), and load current loop (36). While there certainly may exist some minor current loops in the actual circuit of the present invention, they are not significant —— that is they do not adversely affect performance in the desired regimes —— in the manner that the several loops of the

prior art do. Thus the present invention has only one significant current loop and its design acts to minimize any undesirable circulating currents and current loops.

It should also be understood that lead inductances (32) are internal to the transistor as well as external, so only a portion of it may be controlled. Potentially harmful circulating currents will be generated through the switch as a result of this additional loop. This is especially true at high power levels where the maximum possible output power will be limited due to excessive currents through the switch. This effect is, of course, also more significant as the frequency is raised. Although the addition of another loop in the circuit may not be significant at low power levels, it can become a limiting factor at higher power levels. Conversely, without external capacitor (42), lead inductances (32) may simply be included in the series inductance value required in the conditioning circuitry. Instead of adding the additional component of external capacitor (42), the present invention affirmatively utilizes varactor capacitor (38) to achieve its function.

By use of hybrid technology to manufacture switch (13), a fixed capacitor could of course be placed immediately adjacent to the die, reducing the inductance between the internal die capacitance and the external fixed capacitance (the latter is not shown schematically). Although this will significantly lessen the effect of the undesired switch current loop (34), other power limiting problems will result from the interconnect required to parallel the fixed capacitor across the die.

As mentioned earlier, FETs are often used as switching transistors. As a consequence of their construction these include reverse diode (41). This element is actually a parasitic bipolar transistor which is forward biased when the output voltage drops below the common voltage reference. Stress on, even failure of, this transistor (acting in essence as reverse diode (41)) can result if the rate of voltage rise across the device (dv/dt) exceeds the capability of the transistor. In general, for Class E amplifiers, this type of stress can be ignored since the output power or fundamental frequency of operation is low, and therefore the rate of change of voltage across the device rarely approaches this limitation. As either power or frequency is increased, however, this aspect can become important and even

limiting. The dv/dt stress can limit the output power enabled by the FET switch by limiting the output voltage that the transistor is capable of generating reliably.

The dv/dt rating of a device is usually broken up into two different categories, static and commutating dv/dt. The static dv/dt rating applies when the internal diode is reverse biased. The commutating dv/dt rating results from applying reverse bias to the diode before it has had time to fully recover from a previous forward bias condition. In present devices, the static dv/dt capability is approximately three to four times greater than the commutating dv/dt capability. For maximum output voltage across a given FET at a frequency which is high enough to risk stressing a device due to the dv/dt limit, it is critical that the device's output voltage remain at or above the common voltage reference to avoid forward biasing the internal diode and thus taking advantage of the higher static dv/dt rating. If the output voltage falls below the common voltage reference and forward biases the internal diode, the lower commutating dv/dt rating may be exceeded when the output voltage again rises rapidly across the switch.

In understanding the synergistic advances which together combine to allow the performance improvements of the present invention, it is important to note that utilization of varactor capacitor (38) as the capacitor element required across the switch in the switch-mode RF amplifier circuitry will reduce the dv/dt stress by approximately 20% for the same peak voltage across the device. This is also significant when trying to achieve higher power levels at high frequencies.

Despite the prior teachings and preconceptions, the present invention achieves a reduction in the effects that varactor capacitor (38) has on the peak voltage ratio by allowing the output voltage level just prior to the start of conduction to remain substantially higher than zero, even to levels greater than 20% of the supply voltage. This voltage step, which was found in one embodiment to offer the most optimum set of conditions at 50% of the supply voltage, addresses several of the concerns raised when no fixed external capacitor (42) is placed in parallel with varactor capacitor (38).

An advantage derived from the introduction of voltage step (24) is that if desired, maximum response voltage (47) can be decreased. When voltage step (24) is equal to approximately 50% of the supply voltage, it has been found that the peak voltage and output power are reduced in possibly an optimum manner from that of the prior art Class E amplifier. Conversely, when the supply voltage is then increased so the peak voltage of the waveform with the step is returned to the maximum capability of the peak voltage of the prior art Class E amplifier, the resulting output power for the same approximate loading is notably greater. In this manner, the components of network current loop (33) and power supply (12) act as a means for maximizing or increasing the power output of the amplifier while maintaining the same maximum response voltage (47) on switch (13). In assessing the optimum ratio or value of voltage step (24), it should be understood that theoretical understanding has not yet been developed, thus broad variation may be desirable. While at present, it is believed that a value of approximately 50% of the supply voltage represents an optimum value, it is also believed that some advantages can be achieved with a smaller, but still substantial voltage step, namely one in which the losses would be considered significant and undesirable by those skilled in the prior art. At present it is also believed that meaningful improvements in performance exist at values above about the 20% level. How closely this level is determined will, of course, be determined by the level at which improved performance is possible for the particular application.

Allowing for a substantial voltage step across the switch immediately prior to conduction also prevents the possibility of forward biasing the FET internal diode, increasing the effective dv/dt stress capability. The optimum Class E amplifier creates a positive voltage waveform across the switch when the switch is off that is substantially sinusoidal prior to the start of conduction, and which decays at a zero slope to zero volts at the start of conduction. Tuning for this type of waveform has been taught in the prior art to be critical. Since harmonic currents flow in most practical circuitries, the waveform prior to conduction can produce a slightly non-zero voltage and/or non-zero slope waveform. If the voltage across the switch even slightly reverses and allows the internal reverse diode to conduct, and if the reverse recovery time of the internal diode is greater than the

time of conduction, then upon turn-off of the transistor the rising voltage across the transistor will cause the diode to commutate, and the resulting lessened dv/dt capability of the device may cause a failure in the transistor long before maximum voltage limitations become important.

This effect can also be caused in other ways. Since the shape of both response voltage waveform (46) and Class E voltage waveform (17) are both fairly sensitive to the load, a slightly changing load impedance can cause the waveform of a prior art Class E amplifier to swing below zero, again causing the internal diode to conduct with the associated loss in dv/dt rating and possible failure of the device. By allowing a substantial voltage step (24) just prior to the start of conduction, response voltage waveform (46) is assured to be positive, even during slight load variations, therefore decreasing the possibility of dv/dt failure of switch (13). As mentioned earlier, the problem of device failure due to the voltage rise during diode commutation is particularly important at higher power levels. Operating the circuit at higher frequencies also increases the dv/dt across the switch, making the need to avoid forward biasing of reverse diode (41) also important in this case. Switch (13) is of course less likely to experience failure at lower power levels or lower frequencies.

As mentioned earlier, at the initiation of conductive time period (30), the voltage across switch (13), and therefore across varactor capacitor (38), will discharge quickly creating some turn-on switching losses. This can be calculated as approximately $\frac{1}{2}CV_{step}^2f$, where C is the capacitance at V_{step}, the final voltage prior to turn-on, and f is the operating frequency. This produces a current spike through the switch which can be much higher than the nominal peak current through the switch. Since the switching time of the switch is not zero, the peak of the current spike will not exceed the peak current ratings of a properly selected device, and the temperature rise of the switch due to the high momentary current can be made to be insignificant due to the short time it takes the circuit to discharge varactor capacitor (38). In contrast to the teaching of the prior art, it has been found that these step losses attribute only a small drop in efficiency, perhaps only a few percent. However, to compensate for this loss, it has been

discovered that the addition of voltage step (24) has the effect of lowering the average current through the switch thus lowering conduction losses for the same conduction angle. This reduction of conduction losses does not theoretically entirely make up for the additional losses incurred in the switch itself. However, in practice, experimental amplifier circuits have shown little overall change in efficiency when the step is introduced. In fact, improved efficiency has been demonstrated by introduction of the voltage step. This may be surprising to those skilled in the prior art because of their concentration on losses in the switch element itself. The lower average current in the circuit reduces the losses in the other circuit elements by amounts more than enough to compensate for the slightly increased switch losses resulting in the observed increase in efficiency.

The teachings of the prior art also stressed the importance of maintaining exactly 180 degree conduction angles. In fact, when voltage step (24) is incorporated, the conduction angle may be adjusted below 180 degrees to optimize the voltage and current stresses presented to switch (13). As the conduction angle is decreased, the peak current through the switch is increased while at the same time the peak voltage across switch (13) is decreased. Naturally, different switches may display different optimum conduction angles. When coordinated with the supply voltage of voltage supply (12), varactor capacitance (38), reactive network circuitry (15), and load (11), a higher power may be obtained by adjusting the conduction angle below 180 degrees. The particular electrical characteristics of switch (13) may determine the optimum conduction angle.

One of the important aspects of switch (13) when used for the generation of high power RF energy is the relationship between its varactor capacitor (38) and its maximum output voltage rating. For high voltage FET's, varactor capacitor (38) (otherwise known as output capacitance, drain to source capacitance, or Coss) measured at any particular drain and gate voltages is primarily a function of die size with a less strong relationship to breakdown voltage —— the voltage above which the switch will either fail or become unreliable. Naturally for the present invention, a higher breakdown voltage together with higher output capacitance is desired for higher power operation. To achieve improved performance, a substantial varactor

capacitor (38) may be selected. By substantial, it is meant that rather than selecting switch (13) in a manner which minimizes the value of this component, the switch would actually be selected for the highest value in relation to the trade-offs possible in the breakdown voltage and other aspects. Surprisingly, it has been found that even switches with breakdown voltages above a level at which RF utilization was previously assumed to be inappropriate —— about a 400 volt level —— work well in the present invention. In considering such breakdown levels, it should be understood that not just manufacturer's specifications can be relied upon with respect to this aspect. Rather, the switch's actual function is the key aspect since ratings are often based upon considerations beyond actual performance.

In the circuit of the invention, only the internal varactor capacitance of the switch itself is used for the tuning of the output circuit. For a given frequency of operation, conduction angle, and specific transistor type, the value of varactor capacitor (38) and the maximum allowable output switch voltage or breakdown voltage will determine all other parameters of the output circuit, including inductor value, series capacitor value, load resistance, maximum supply voltage, and output power. Thus each of these are uniquely coordinated to the internal capacitance of switch (13) and selection of switch (13). The internal capacitance of switch (13) acts to establish the parameters of frequency and power optimally possible.

It is the nature of amplifiers of this type that the output power varies as the square of the supply voltage, while the output impedances usually vary directly with the output capacitance. This makes simple scaling to achieve higher powers a difficult task. To apply the teachings of the present invention, consider the possibility of increasing the power of a typical amplifier operating with a maximum swing of 80 volts on a 100 volt transistor producing an output power of 200 watts with an efficiency of 90% by replacement of the output transistor with a 1000 volt transistor with approximately the same die size. For a typical FET the output capacitance would decrease approximately four times due to the change in voltage rating. For the same class of operation this would typically also result in all impedances being scaled up by four times. Without an increase in supply voltage, this factor would cause the output power to initially be decreased by four times,

not increase as desired. Since now the power supply voltage could be increased by 10 times causing a power increase of 100 times, the final circuit with both voltage level and impedance changes would therefore theoretically allow an output capacity of about 5000 watts. Obviously there are smaller incremental steps of increased voltage and power, but each step represents a significant power increase with all of the attendant problems to solve.

To reach such high power levels several problems must be simultaneously solved, however. These include dealing with increased power dissipation, dv/dt switch limits, layout, and parasitic loops. The method and circuit of the invention provide solutions for attaining such previously unattainable power levels from this simple circuit whenever the appropriate switch is available.

To achieve the performance improvements, one embodiment of the invention uses available packaged FETs. In this embodiment it is important that several small die type devices be used and mounted in a symmetrical configuration with the most compact layout possible. Another embodiment of the invention uses a hybrid module containing several small FET dice, with drain-to-source ratings between 400 volts and 1000 volts. Naturally, the higher voltage dice enable the circuit to yield higher powers. In either case, there is a unique relationship between output capacitance and maximum output power which can be obtained by coordination of the circuit element values as described earlier.

In the preferred experimental circuit, the topology appears nearly identical to many series resonant circuits such as mixed-mode Class C or Class E RF amplifiers. The distinctive elements are the drive, conduction angle, voltage waveforms, switch type, and output circuit values. These together act to produce very different operational modes and very improved performance. The drive circuit is designed to provide five to ten amps rms into a capacitive load. In the experimental test circuit an "L" network was used on the output to transform the load impedance to about 50 ohms.

The foregoing discussion and the claims which follow describe the preferred embodiments of the present invention. Particularly with respect to the claims, it should be understood that changes may be made without departing from its essence. In this regard, it is intended that such changes would still fall within the scope of the present invention. It simply is not practical to describe and claim all possible revisions to the present invention which may be accomplished. To the extent such revisions utilize the essence of the present invention, each naturally fall within the breadth of protection encompassed by this patent. This is particularly true for the present invention since its basic concepts and understandings are fundamental in nature and can be broadly applied.

CLAIMS

We claim:

1. A method of producing high power radio frequency signals from a switch-mode power amplifier to power a load comprising:
   a. providing a supply voltage to a switch having internal capacitance and capable of rapidly transitioning from a conductive state to a non-conductive state; while
   b. causing said switch to rapidly transition to its conductive state and to remain conductive for a conductive time period during which said supply voltage causes current to flow through said switch; then
   c. conditioning the current flowing through said switch by reactive network circuitry during said conductive time period; then
   d. causing said switch to rapidly transition to its non-conductive state and remain non-conductive for a response time period during which voltage appears across said switch; then
   e. creating a response voltage waveform through action of said reactive network circuitry, wherein said reactive network circuitry affirmatively utilizes the internal capacitance of said switch without being affected by a shunt capacitor, and wherein said response waveform has a time-varying voltage throughout said response time period; then
   f. again causing said switch to rapidly transition to its conductive state at a turn-on time and thus recommencing the conduction time period wherein the voltage immediately prior to said turn-on time is substantial.

2. A method of producing high power radio frequency signals from a switch mode power amplifier as described in claim 1 wherein said switch has internal capacitance and wherein said internal capacitance of said switch comprises an internal varactor capacitance.

3. A method of producing high power radio frequency signals from a switch mode power amplifier as described in claim 2 wherein said internal varactor capacitance is substantial.

4. A method of producing high power radio frequency signals from a switch mode power amplifier as described in claim 3 wherein said switch has a breakdown voltage and wherein said breakdown voltage is not less than 400 volts.

5. A method of producing high power radio frequency signals from a switch mode power amplifier as described in claim 1 wherein the voltage of said response waveform at said turn-on time is approximately 50% of said supply voltage.

6. A method of producing high power radio frequency signals from a switch mode power amplifier as described in claim 1 or 3 wherein the voltage of said response waveform at said turn-on time is greater than 20% of said supply voltage.

7. A method of producing high power radio frequency signals from a switch mode power amplifier as described in claim 1 wherein said time-varying voltage of said response waveform is always positive.

8. A method of producing high power radio frequency signals from a switch mode power amplifier as described in claim 1 wherein said reactive network circuitry is uniquely coordinated with the internal capacitance of said switch.

9. A method of producing high power radio frequency signals from a switch mode power amplifier as described in claim 1 wherein said power amplifier has a desired frequency of operation, wherein said reactive network circuitry comprises an inductor, a separate capacitor, and said load and further comprising the step of coordinating said inductor, separate capacitor, load, supply voltage, and desired frequency of operation to the internal capacitance of said switch throughout said response time period.

10. A method of producing high power radio frequency signals from a switch mode power amplifier as described in claim 9 wherein said step of

coordinating said inductor, separate capacitor, load, supply voltage, and desired frequency of operation to the internal capacitance of said switch throughout said response time period further comprises the step of selecting said switch to have internal capacitance to establish said desired frequency of operation and said power to said load.

11. A method of producing high power radio frequency signals from a switch mode power amplifier as described in claim 1 wherein said switch has a common lead having voltage and further comprising the step of driving said switch by a radio frequency voltage having an average drive voltage while accomplishing said step of causing said switch to rapidly transition to its conductive state and said step of causing said switch to rapidly transition to its non-conductive state wherein said average drive voltage and the voltage of said common lead are equal.

12. A method of producing high power radio frequency signals from a switch mode power amplifier as described in claim 1 or 11 wherein said power amplifier provides radio frequency power, wherein said switch has particular electrical characteristics and wherein said steps of causing said switch to rapidly transition to its conductive state and causing said switch to rapidly transition to its non-conductive state comprise the step of creating a conduction angle defining the relative durations of said conductive time period and said response time period and further comprising the step of adjusting said conduction angle to optimize said radio frequency power corresponding to said particular electrical characteristics of said switch.

13. A method of producing high power radio frequency signals from a switch mode power amplifier as described in claim 1 wherein said switch has substantial internal capacitance and further comprising the step of minimizing any undesirable circulating currents through said switch prior to accomplishing said step of again causing said switch to rapidly transition to its conductive state at a turn-on time and thus recommencing the conduction time period.

14. A method of producing high power radio frequency signals from a switch mode power amplifier as described in claim 13 wherein said switch has lead inductance and wherein said step of minimizing any undesirable circulating currents comprises the step of affirmatively utilizing the lead inductance of said switch.

15. A method of producing high power radio frequency signals from a switch mode power amplifier as described in claim 14 wherein said power amplifier has a frequency of operation and wherein said step of minimizing any undesirable circulating currents further comprises the step of creating only one significant current loop within said power amplifier wherein said current loop is substantially series resonant at said frequency of operation.

16. A method of producing high power radio frequency signals from a switch mode power amplifier as described in claim 1 or 5 and further comprising the step of minimizing any undesirable circulating currents through said switch while accomplishing said step of creating a response voltage waveform through action of said reactive network circuitry.

17. A method of producing high power radio frequency signals from a switch mode power amplifier as described in claim 1, 3, or 5 wherein said switch has lead inductance and further comprising the step of affirmatively utilizing the lead inductance of said switch during said response time period.

18. A method of producing high power radio frequency signals from a switch mode power amplifier as described in claim 17 wherein said power amplifier has a frequency of operation and further comprising the step of creating only one significant current loop within said power amplifier wherein said current loop is substantially series resonant at said frequency of operation.

19. A high power, switch mode radio frequency power amplifier to provide power to a load comprising:

a. a radio frequency driver;

b. a means for switching having internal capacitance and responsive to said driver wherein said means for switching operates rapidly and is capable of alternatingly establishing a conductive state for a conductive time period and a non-conductive state for a response time period;

c. a means for providing a supply voltage to said switch;

d. a means for conditioning responsive to said supply voltage, wherein said means for conditioning affirmatively utilizes the internal capacitance of said means for switching without being affected by a shunt capacitor, and wherein said means for conditioning acts to create a response voltage waveform wherein said response waveform has a time-varying voltage during said response time period and wherein said response voltage waveform has substantial voltage at the end of said response time period.

20. A high power, switch mode radio frequency power amplifier to provide power to a load as described in claim 19 wherein said means for conditioning comprises only one significant current loop and wherein said significant current loop comprises:

a. said load;

b. an inductive means serially connected to said load;

c. a capacitive means serially connected to said inductive means; and

d. said switch serially connected to said capacitive means.

21. A high power, switch mode radio frequency power amplifier to provide power to a load as described in claim 20 wherein said means for switching comprises an internal capacitive means.

22. A high power, switch mode radio frequency power amplifier to provide power to a load as described in claim 21 wherein said internal capacitive means comprises a varactor capacitor.

23. A high power, switch mode radio frequency power amplifier to provide power to a load as described in claim 22 wherein said varactor capacitor is substantial.

24. A high power, switch mode radio frequency power amplifier to provide power to a load as described in claim 23 wherein said varactor capacitor has a breakdown voltage and wherein said breakdown voltage is not less than 400 volts.

25. A high power, switch mode radio frequency power amplifier to provide power to a load as described in claim 19 or 23 wherein the voltage of said response waveform at said turn-on time is approximately 50% of said supply voltage.

26. A high power, switch mode radio frequency power amplifier to provide power to a load as described in claim 19 or 23 wherein the voltage of said response waveform at said turn-on time is greater than 20% of said supply voltage.

27. A high power, switch mode radio frequency power amplifier to provide power to a load as described in claim 19 wherein said means for switching has a source lead voltage, wherein said supply voltage is referenced to a common voltage reference, and wherein the time-varying voltage of said response waveform is always positive with respect to said common voltage reference.

28. A high power, switch mode radio frequency power amplifier to provide power to a load as described in claim 21 wherein said inductive means and said capacitive means are coordinated with said internal capacitive means.

29. A high power, switch mode radio frequency power amplifier to provide power to a load as described in claim 28 wherein said power amplifier has a desired frequency of operation and wherein said load, said desired

frequency of operation and said supply voltage are coordinated with said internal capacitive means.

30. A high power, switch mode radio frequency power amplifier to provide power to a load as described in claim 29 wherein said switch is selected to have internal capacitance to establish said desired frequency of operation and said power to said load.

31. A high power, switch mode radio frequency power amplifier to provide power to a load as described in claim 19 or 23 wherein said switch has a common lead having voltage, wherein said radio frequency driver creates a radio frequency voltage having an average drive voltage, and wherein said average drive voltage and said common lead voltage are equal.

32. A high power, switch mode radio frequency power amplifier to provide power to a load as described in claim 31 wherein said switch has particular electrical characteristics, wherein said radio frequency driver creates a conduction angle defining the relative durations of said conductive time period and said response time period and wherein said conduction angle is set to optimize the power provided to said load according to said particular electrical characteristics of said switch.

33. A high power, switch mode radio frequency power amplifier to provide a level of power to a load comprising:

a. a radio frequency driver;

b. a means for switching responsive to said driver, wherein said means for switching has internal capacitance, and wherein said means for switching operates rapidly and is capable of alternatingly establishing a conductive state for a conductive time period and a non-conductive state for a response time period;

c. a means for providing a supply voltage to said switch;

d. a means for conditioning responsive to said supply voltage wherein said means for conditioning acts to create a maximum switch voltage during said response time period; and

e. a means for reducing the maximum switch voltage during said response time period while maintaining said level of power to said load wherein said means for reducing affirmatively utilizes the internal capacitance of said means for switching without being affected by a shunt capacitor.

34. A high power, switch mode radio frequency power amplifier to provide power to a load as described in claim 33 wherein said means for reducing the maximum switch voltage during said response time period comprises said means for conditioning.

35. A high power, switch mode radio frequency power amplifier to provide power to a load as described in claim 34 wherein said means for conditioning acts to create a response voltage waveform, wherein said response waveform has a time-varying voltage during said response time period and wherein said response voltage waveform has substantial voltage at the end of said response time period.

36. A high power, switch mode radio frequency power amplifier to provide a level of power to a load comprising:

a. a radio frequency driver;

b. a means for switching responsive to said driver, wherein said means for switching has internal capacitance, and wherein said means for switching operates rapidly and is capable of alternatingly establishing a conductive state for a conductive time period and a non-conductive state for a response time period;

c. a means for providing a supply voltage to said switch;

d. a means for conditioning responsive to said supply voltage wherein said means for conditioning acts to create a maximum switch voltage during said response time period; and

e. a means for increasing said level of power provided to said load without increasing said maximum switch voltage wherein said means for increasing affirmatively utilizes the internal capacitance of said means for switching without being affected by a shunt capacitor.

37. A high power, switch mode radio frequency power amplifier to provide power to a load as described in claim 36 wherein said means for increasing said level of power provided to said load comprises said means for conditioning.

38. A high power, switch mode radio frequency power amplifier to provide power to a load as described in claim 37 wherein said means for conditioning acts to create a response voltage waveform, wherein said response waveform has a time-varying voltage during said response time period and wherein said response voltage waveform has substantial voltage at the end of said response time period.

39. A high power, switch mode radio frequency power amplifier to provide power to a load comprising:

a. a radio frequency driver;

b. a means for switching responsive to said driver wherein said means for switching operates rapidly and is capable of alternatingly establishing a conductive state for a conductive time period and a non-conductive state for a response time period;

c. a means for providing a supply voltage to said switch;

d. a means for conditioning responsive to said supply voltage wherein said means for conditioning acts to create a response voltage waveform, wherein said response waveform has a time-varying voltage during said response time period, wherein said response voltage waveform has substantial voltage at the end of said response time period, wherein said means for conditioning comprises only one significant current loop, and wherein said significant current loop further comprises:

1) said load;

2) an inductive means serially connected to said load;

3) a capacitive means serially connected to said inductive means; and

4) said switch serially connected to said capacitive means.

40. A high power, switch mode radio frequency power amplifier to provide power to a load as described in claim 39 wherein said means for switching comprises an internal capacitive means.

41. A high power, switch mode radio frequency power amplifier to provide power to a load as described in claim 40 wherein said internal capacitive means comprises a varactor capacitor.

42. A high power, switch mode radio frequency power amplifier to provide power to a load as described in claim 41 wherein said varactor capacitor is substantial.

43. A high power, switch mode radio frequency power amplifier to provide power to a load as described in claim 42 wherein said varactor capacitor has a breakdown voltage and wherein said breakdown voltage is not less than 400 volts.

44. A high power, switch mode radio frequency power amplifier to provide power to a load as described in claim 39 or 42 wherein the voltage of said response waveform at said turn-on time is approximately 50% of said supply voltage.

45. A high power, switch mode radio frequency power amplifier to provide power to a load as described in claim 39 or 42 wherein the voltage of said response waveform at said turn-on time is greater than 20% of said supply voltage.

46. A high power, switch mode radio frequency power amplifier to provide power to a load as described in claim 39 wherein said means for switching has a source lead voltage, wherein said supply voltage is referenced to a common voltage reference, and wherein the time-varying voltage of said response waveform is always positive with respect to said common voltage reference.

47. A high power, switch mode radio frequency power amplifier to provide power to a load as described in claim 40 wherein said inductive means and said capacitive means are coordinated with said internal capacitive means.

48. A high power, switch mode radio frequency power amplifier to provide power to a load as described in claim 47 wherein said power amplifier has a desired frequency of operation and wherein said load, said desired frequency of operation and said supply voltage are coordinated with said internal capacitive means.

49. A high power, switch mode radio frequency power amplifier to provide power to a load as described in claim 48 wherein said switch is selected to have internal capacitance to establish said desired frequency of operation and said power to said load.

50. A high power, switch mode radio frequency power amplifier to provide power to a load as described in claim 39 or 42 wherein said switch has a common lead having voltage, wherein said radio frequency driver creates a radio frequency voltage having an average drive voltage, and wherein said average drive voltage and said common lead voltage are equal.

51. A high power, switch mode radio frequency power amplifier to provide power to a load as described in claim 50 wherein said switch has particular electrical characteristics, wherein said radio frequency driver creates a conduction angle defining the relative durations of said conductive time period and said response time period and wherein said conduction angle is

set to optimize the power provided to said load according to said particular electrical characteristics of said switch.

52. A method of producing high power radio frequency signals from a switch-mode power amplifier to power a load comprising:

a. providing a supply voltage to a switch having internal capacitance and capable of rapidly transitioning from a conductive state to a non-conductive state; while

b. causing said switch to rapidly transition to its conductive state and to remain conductive for a conductive time period during which said supply voltage causes current to flow through said switch; then

c. conditioning the current flowing through said switch by reactive network circuitry during said conductive time period; then

d. causing said switch to rapidly transition to its non-conductive state and remain non-conductive for a response time period during which voltage appears across said switch; then

e. creating a response voltage waveform through action of said reactive network circuitry, and wherein said response waveform has a time-varying voltage throughout said response time period; then

f. again causing said switch to rapidly transition to its conductive state at a turn-on time and thus recommencing the conduction time period wherein the voltage immediately prior to said turn-on time is substantial.

53. A high power, switch mode radio frequency power amplifier to provide power to a load comprising:

a. a radio frequency driver;

b. a means for switching responsive to said driver wherein said means for switching operates rapidly and is capable of alternatingly establishing a conductive state for a conductive time period and a non-conductive state for a response time period;

c. a means for providing a supply voltage to said switch;

d. a means for conditioning responsive to said supply voltage wherein said means for conditioning acts to create a response voltage waveform wherein said response waveform has a time-varying voltage during said response time period and wherein said response voltage waveform has substantial voltage at the end of said response time period.

54. A high power, switch mode radio frequency power amplifier to provide a level of power to a load comprising:

a. a radio frequency driver;

b. a means for switching responsive to said driver wherein said means for switching operates rapidly and is capable of alternatingly establishing a conductive state for a conductive time period and a non-conductive state for a response time period;

c. a means for providing a supply voltage to said switch;

d. a means for conditioning responsive to said supply voltage wherein said means for conditioning acts to create a maximum switch voltage during said response time period; and

e. a means for reducing the maximum switch voltage during said response time period while maintaining said level of power to said load.

55. A high power, switch mode radio frequency power amplifier to provide a level of power to a load comprising:

a. a radio frequency driver;

b. a means for switching responsive to said driver wherein said means for switching operates rapidly and is capable of alternatingly establishing a conductive state for a conductive time period and a non-conductive state for a response time period;

c. a means for providing a supply voltage to said switch;

d. a means for conditioning responsive to said supply voltage wherein said means for conditioning acts to create a maximum switch voltage during said response time period; and

e. a means for increasing said level of power provided to said load without increasing said maximum switch voltage.

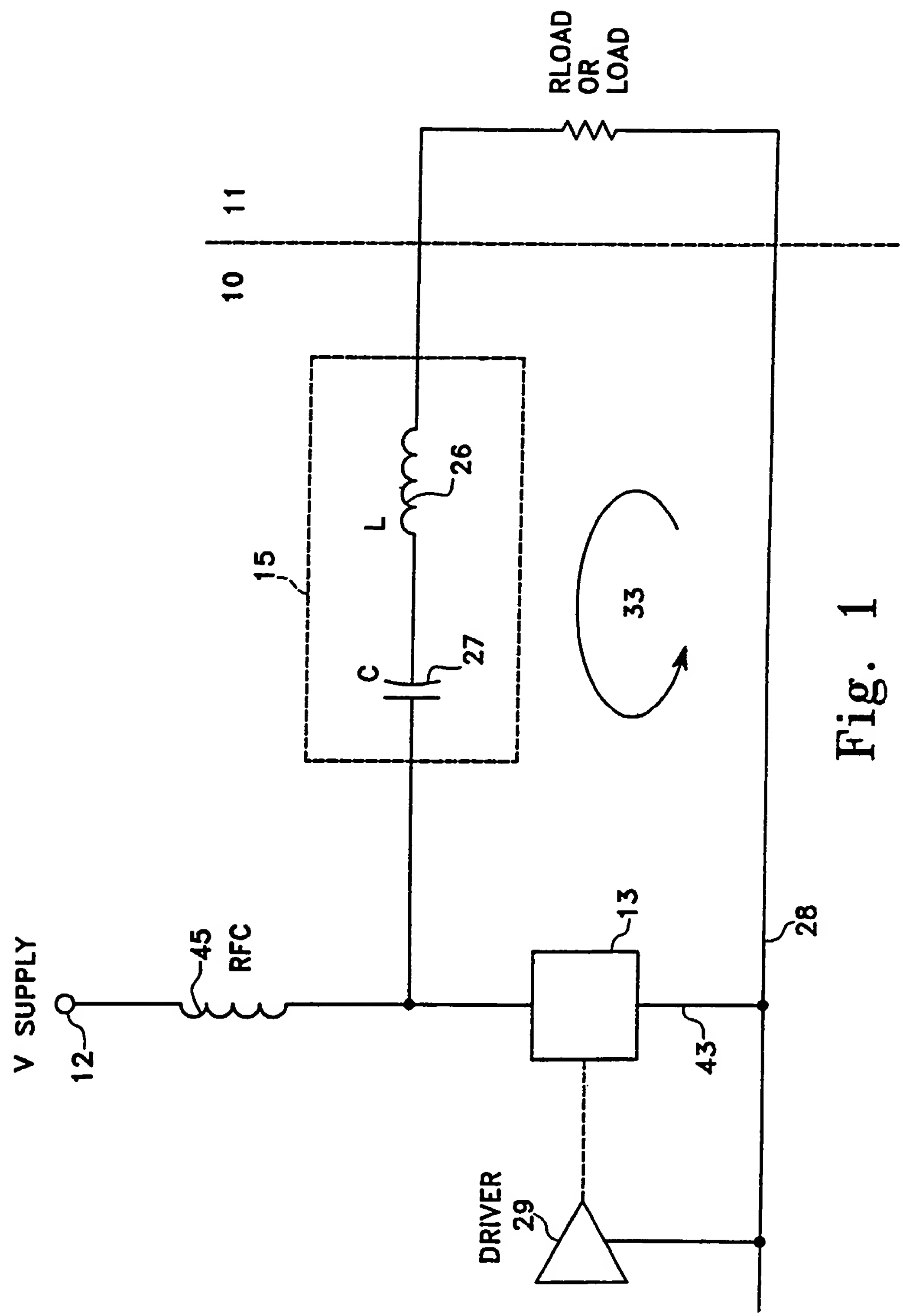

RLOAD
OR
LOAD
11
10
15
26
L
C
27
33
V SUPPLY
12
45
RFC
13
28
43
DRIVER
29

Fig. 1

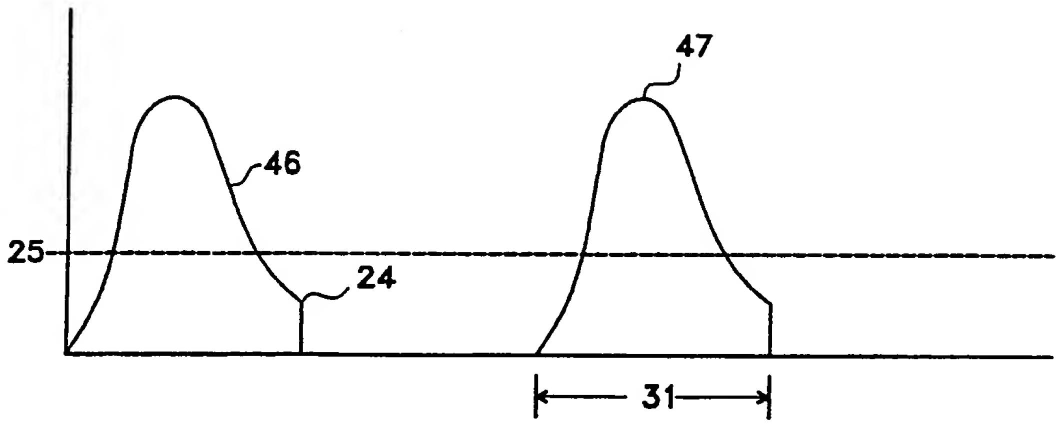


Fig. 2a

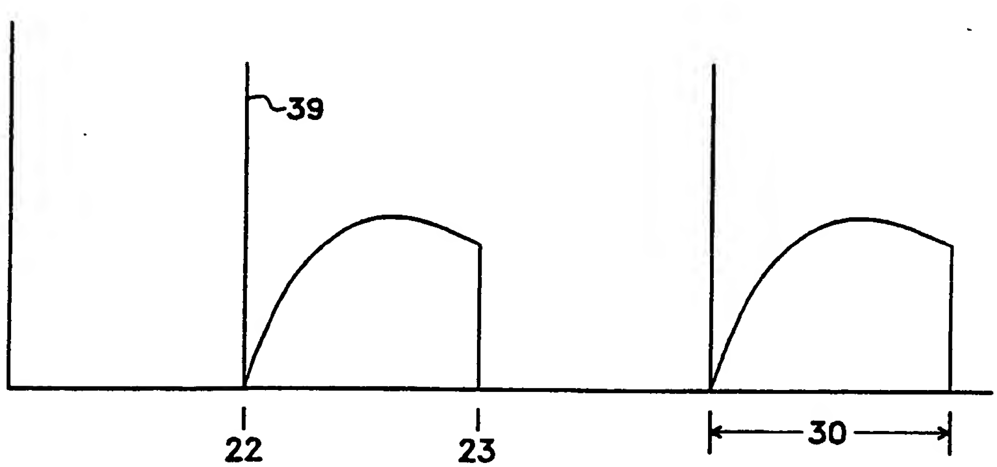


Fig. 2b

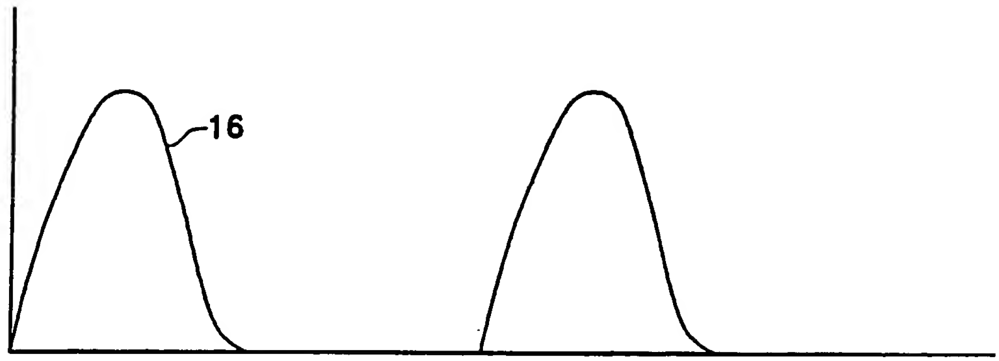


Fig. 3a

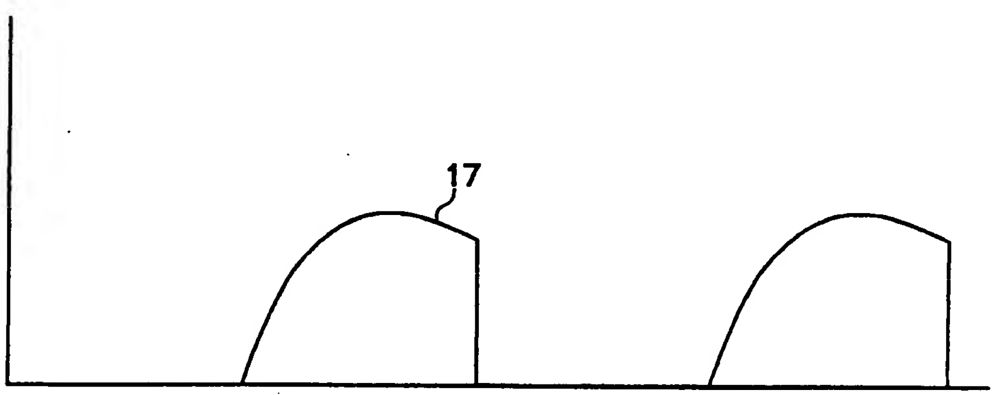


Fig. 3b

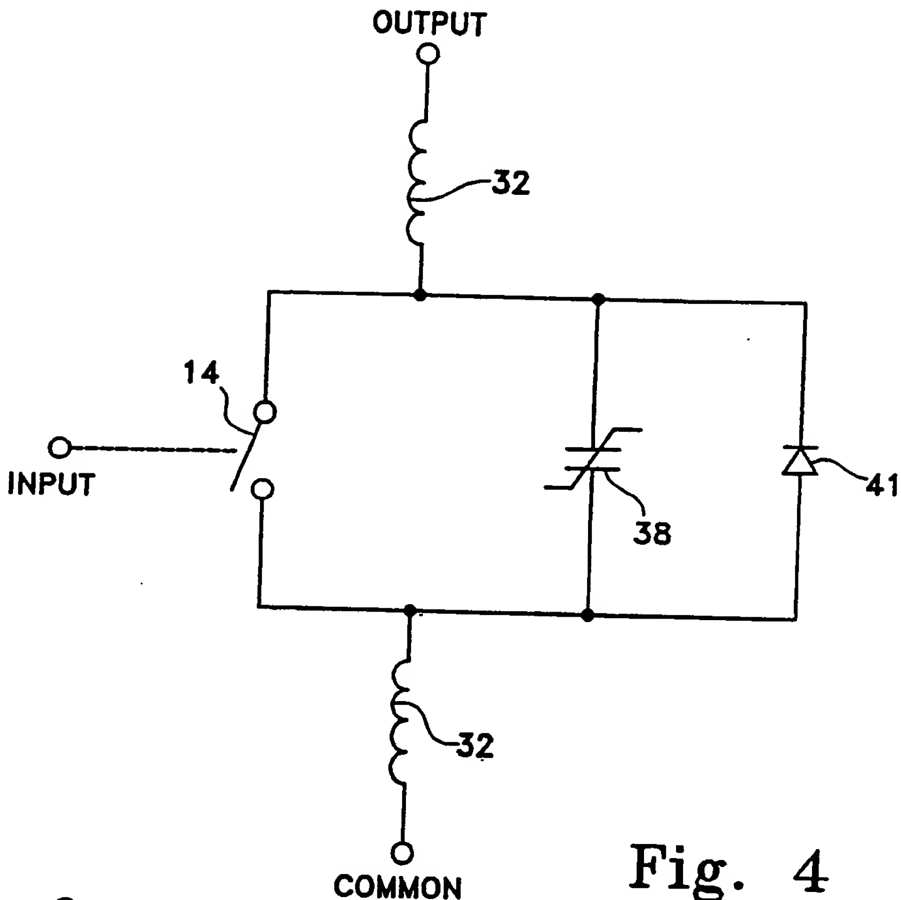


Fig. 4

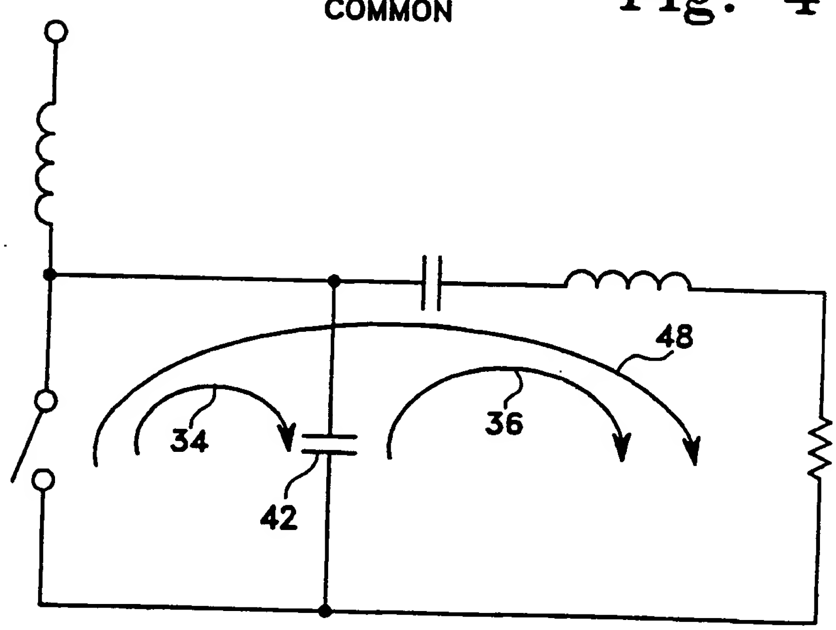


Fig. 5

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 92/00844

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl. 5 H03F3/217

II. FIELDS SEARCHED

Minimum Documentation Searched[7]

Classification System	Classification Symbols
Int.Cl. 5	H03F ; H02M

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched[8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category °	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No.[13]
A	US,A,4 891 746 (W.C. BOWMAN ET AL) 2 January 1990 cited in the application see the whole document ---	1-55
A	US,A,4 449 174 (N.G. ZIESSE) 15 May 1984 cited in the application see the whole document ---	1-55
A	IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS. vol. 37, no. 8, August 1990, NEW YORK US pages 1057 - 1060; J.C. MANDOJANA ET AL: 'A DISCRETE/CONTINUOUS TIME-DOMAIN ANALYSIS OF A GENERALIZED CLASS E AMPLIFIER' see the whole document ---	1-55

° Special categories of cited documents : [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
09 JUNE 1992	12 JUN 1992
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	TYBERGHIEN G.M.

1

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO. US 9200844 SA 57020

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 09/06/92 The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US-A-4891746	02-01-90	CA-A- 1295671	11-02-92
		EP-A- 0372792	13-06-90
		JP-A- 2246770	02-10-90
US-A-4449174	15-05-84	CA-A- 1212719	14-10-86
		DE-A- 3376174	05-05-88
		EP-A,B 0114466	01-08-84
		GB-A,B 2131235	13-06-84
		JP-A- 59106876	20-06-84

PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 7 : **H03F 3/217, H04B 1/04**	**A1**	**(11) International Publication Number:** **WO 00/64044** **(43) International Publication Date:** 26 October 2000 (26.10.00)

(21) International Application Number: PCT/EP00/03203

(22) International Filing Date: 11 April 2000 (11.04.00)

(30) Priority Data:
99201195.7 19 April 1999 (19.04.99) EP

(71) Applicant *(for all designated States except US)*: SEMICONDUCTOR IDEAS TO THE MARKET (ItoM) B.V. [NL/NL]; Drielindendreef 53, NL-4389 AH Breda (NL).

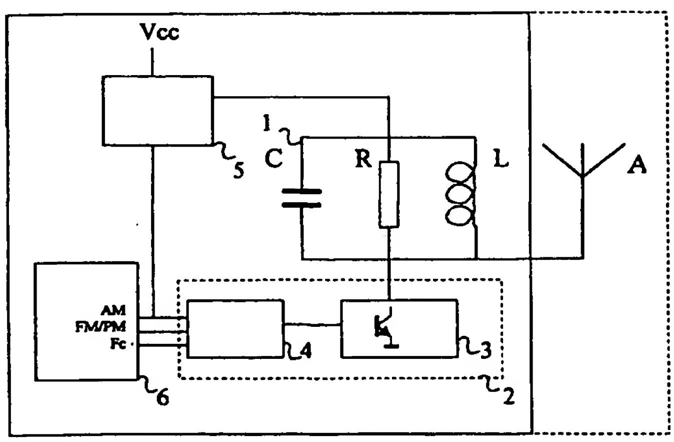
(72) Inventor; and
(75) Inventor/Applicant *(for US only)*: VAN RUMPT, Herman, Wouter [NL/NL]; Neercanne 15, NL-5235 HC s'Hertogenbosch (NL).

(74) Agent: VAN STRAATEN, Joop; Octrooibureau van Straaten B.V., Waalreseweg 17, NL-5554 HA Valkenswaard (NL).

(81) Designated States: JP, US, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.

(54) Title: COMMUNICATION DEVICE



(57) Abstract

A communication device including a power amplifier for amplifying a modulated high frequency carrier input signal comprising a resonance circuit and an excitation circuit for a signal excitation in the resonance circuit phase and/or frequency coupled with the modulated high frequency carrier signal. To improve the performance of such communication device a new principle having an efficiency, substantially higher than achievable with the above known power amplifier is based on a reduction of the overall power loss and is achieved by said having excitation occurred within excitation periods (Tex) in a periodic alternation with resonation periods (Tfre), during which the resonance circuit is in a free running resonance mode, the excitation periods being smaller than the resonation periods to define an excitation duty cycle (Tex/Tcar) relative to the period of the carrier signal (Tcar) of less than 0.5. Preferably the resonance frequency (fres) of the resonance circuit is higher than the carrier frequency (fcar) of the modulated high frequency carrier signal over a resonance frequency detuning rate (dfres), defined by the frequency deviation of said resonance frequency from said carrier frequency relative to the carrier frequency (fres/fcar−1), substantially at most corresponding to half the excitation duty cycle.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania
AM	Armenia
AT	Austria
AU	Australia
AZ	Azerbaijan
BA	Bosnia and Herzegovina
BB	Barbados
BE	Belgium
BF	Burkina Faso
BG	Bulgaria
BJ	Benin
BR	Brazil
BY	Belarus
CA	Canada
CF	Central African Republic
CG	Congo
CH	Switzerland
CI	Côte d'Ivoire
CM	Cameroon
CN	China
CU	Cuba
CZ	Czech Republic
DE	Germany
DK	Denmark
EE	Estonia
ES	Spain
FI	Finland
FR	France
GA	Gabon
GB	United Kingdom
GE	Georgia
GH	Ghana
GN	Guinea
GR	Greece
HU	Hungary
IE	Ireland
IL	Israel
IS	Iceland
IT	Italy
JP	Japan
KE	Kenya
KG	Kyrgyzstan
KP	Democratic People's Republic of Korea
KR	Republic of Korea
KZ	Kazakstan
LC	Saint Lucia
LI	Liechtenstein
LK	Sri Lanka
LR	Liberia
LS	Lesotho
LT	Lithuania
LU	Luxembourg
LV	Latvia
MC	Monaco
MD	Republic of Moldova
MG	Madagascar
MK	The former Yugoslav Republic of Macedonia
ML	Mali
MN	Mongolia
MR	Mauritania
MW	Malawi
MX	Mexico
NE	Niger
NL	Netherlands
NO	Norway
NZ	New Zealand
PL	Poland
PT	Portugal
RO	Romania
RU	Russian Federation
SD	Sudan
SE	Sweden
SG	Singapore
SI	Slovenia
SK	Slovakia
SN	Senegal
SZ	Swaziland
TD	Chad
TG	Togo
TJ	Tajikistan
TM	Turkmenistan
TR	Turkey
TT	Trinidad and Tobago
UA	Ukraine
UG	Uganda
US	United States of America
UZ	Uzbekistan
VN	Viet Nam
YU	Yugoslavia
ZW	Zimbabwe

Communication device

The invention relates to a communication device including a power amplifier for amplifying a modulated high frequency carrier input signal comprising a resonance circuit and an excitation circuit for a signal excitation in the resonance circuit phase and/or frequency coupled with the modulated high frequency carrier signal.

A communication device including a power amplifier of the above type is known from the article "A 1.9 GHz 1W CMOS Class E Power Amplifier for Wireless Communications" by King-Chun Tsai and Paul R. Gray, Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, California, U.S.A., published in Proceedings of the 24th European Solid-State Conference, The Hague, The Netherlands, 22-24 September 1998.

The resonance circuit of the known power amplifier comprises a parallel LC resonance circuit AC serially connected between a supply voltage terminal and mass, through a controllable switching. The switching element is to switch the full supply voltage across the resonance circuit alternately during half period cycles of the carrier frequency, synchronised with the phase and/or frequency modulation of said high frequency carrier input signal. This results in a likewise synchronised signal excitation in the resonance circuit. The common node between the capacitor and the inductor provides an output of the resonance circuit, and therewith an output of the power amplifier, supplying the information embedded in the modulation with a power amplification to a bandpass filter. The bandpass filter is to select the fundamental component of the voltage occurring across the resonance circuit and to suppress harmonic distortion occurring in the output signal of the resonance circuit.

The resonance circuit is designed such with regard to the switching operation, that in steady state, ideally the resonance circuit signal, i.e. the voltage across the capacitor, crosses zero level, immediately before the switch is closed. According to the teachings of said article, the switch would dissipate no power then, because it is closed when the voltage across the switch is zero, hereinafter also referred to as soft switching concept. The signal losses in the switch, hereinafter also referred to as switching or excitation losses, would therewith be eliminated and all of the DC supply power would therewith be delivered to the output of the LC load network. The measures mentioned to arrive at this ideal situation of zero excitation losses are aimed at an

accurate half cycle periodic operation of the switch, which would a.o. result in the capacitor being fully discharged at the moment the switch is closed, and are aimed at steep switching transients. The circuitry needed for such precise switching operation are rather complex.

However, communication devices have to keep up with ever increasing market demands. Power amplifiers are one of the key circuits basically determining the overall performance of such devices. For important applications within the field of telecommunication, the requirements put to power amplifiers in terms of power added efficiency and cost effectiveness already increased beyond the limits attainable with power amplifiers based on the above known principle.

Therefore, the invention has for its first object to improve the performance of communication devices by providing a power amplifier based on a new principle having an efficiency, substantially higher than achievable with the above known power amplifier.

A second object of the invention is to provide a versatile power amplifier applicable in communication devices complying with a broad range of telecommunication standards.

A third object of the invention is to provide a communication device to great extent being suitable for a cost effective implementation in integrated form.

According to the invention a communication device including a power amplifier for amplifying a modulated high frequency carrier input signal comprising a resonance circuit and an excitation circuit for a signal excitation in the resonance circuit phase and/or frequency coupled with the modulated high frequency carrier signal, is therefore characterized by said excitation occurring within excitation periods (Tex) in a periodic alternation with resonation periods (Tfre), during which the resonance circuit is in a free running resonance mode, the excitation periods being smaller than the resonation periods to define an excitation duty cycle (Tex/Tcar) relative to the period of the carrier signal (Tcar), hereinafter also indicated as excitation duty cycle, of less than 0.5.

Unlike the teachings and aims of the above cited reference, the invention is targeted at a reduction of the overall signal power loss in the total transmitter end stage signal processing including the amplification, selection and transmission of the RF signal. The invention is based on the recognition that extending the free running period of the resonance circuit (Tfre) of the power amplifier beyond a half cycle period results in a reduction of the total harmonic signal distortion,

hereinafter also referred to as THD losses, at the output the resonance circuit without necessarily increasing significantly the above excitation losses. The power needed for an effective signal excitation in the resonance circuit can therefore be reduced as well, without affecting the amplifier output power. This results in an increase in the overall efficiency of the power amplifier.

The invention therewith cuts across the notion that decreasing the duty cycle of a resonance circuit input signal below 0.5 of the signal period will lead to signal power loss due to spectral power spread inherent to any decrease in signal duty cycle.

The measure according to the invention provides a fundamental breakthrough beyond the bottom limit of signal power loss of the known power amplifier, allowing to substantially improve the performance of communication devices.

According to a further recognition of the invention, said measure does not prevent to apply the abovementioned soft switching concept to eliminate excitation losses completely. Starting from a certain excitation duty cycle, a complete elimination of switching losses can be achieved by a certain value for the resonance frequency (fres) of the resonance circuit. On the other hand, by chosing the resonance frequency (fres) of the resonance circuit at the fres at the carrier frequency (fcar) of the modulated high frequency carrier signal THD losses are eliminated. In practise said certain value for the resonance frequency (fres) deviates from the carrier frequency (fcar). Expressing said resonance frequency (fres) in a socalled resonance frequency detuning rate (dfres), defining the frequency deviation by which the resonance frequency (fres) is higher than the carrier frequency (fcar) of the modulated high frequency carrier signal relative to said carrier frequency (dfres=fres/fcar-1), an advantangeous trade off between excitation losses and THD losses according to the invention to come to a minimisation of the overall power loss of the power amplifier as a whole, is met in a preferred embodiment of a communication device according to the invention, which is characterized by said resonance frequency detuning rate (dfres) corresponding substantially at most to half the excitation duty cycle.

This measure allows minor excitation losses to occur, which on the one hand are sufficiently small not to deteriorate the overall reduction in signal power loss of the power amplifier due to the reduction in THD losses, and which on the other hand are sufficiently large to allow for a cost effective implementation, using much less complex circuitry than needed in the cited known power amplifier.

In particular for an excitation duty cycle between an order of magnitude of 0.1 and 0.5, the latter embodiment of a communication device according to the invention is characterized by said resonance frequency detuning rate (dfres) being in the order of magnitude of the half square value of said excitation duty cycle.

Apart from the excitation duty cycle and the resonance frequency detuning rate, also the quality factor (Q) of the resonance circuit is a parameter in the trade off between excitation and THD losses. In a preferred embodiment of a communication device according to the invention using the quality factor as an additional parameter, the excitation duty cycle is being defined to decrease with increasing quality factor (Q) of the resonance circuit and vice versa, in particular for an excitation duty cycle between an order of magnitude of 0.1 and 0.5.

The above measures are approximations of the following, more precise definitions for the abovementioned excitation duty cycle (Tex/Tcar) and resonance frequency detuning rate (dfres), leading to an optimal trade off between excitation losses and THD losses, being substantially equal to:

$$dfres[Q]=0.5\left[\frac{\mathrm{Sqrt}\left[1-\left(1-\frac{1}{Q}\right)^{4}\right]}{2\,\mathrm{Pi}\left(1-\frac{1}{Q}\right)^{2}}+\frac{3+\dfrac{2\,\mathrm{ArcSin}\left[\left(1-\frac{1}{Q}\right)^{2}\right]}{\mathrm{Pi}}}{4}-1\right]$$

and

$$(Tex/Tcar)[Q] = \frac{\mathrm{Sqrt}\left[1 - \left(1 - \frac{1}{Q}\right)^4\right]}{2\,\mathrm{Pi}\left(1 - \frac{1}{Q}\right)^2 \left(\frac{\mathrm{Sqrt}\left[1 - \left(1 - \frac{1}{Q}\right)^4\right]}{2\,\mathrm{Pi}\left(1 - \frac{1}{Q}\right)^2} + \frac{3 + \frac{2\,\mathrm{ArcSin}\left[\left(1 - \frac{1}{Q}\right)^2\right]}{\mathrm{Pi}}}{4} \right)}$$

The trade off between excitation and THD losses according to the invention causes a discontinuity to occur in the slope of the output signal of the resonance circuit during the resonation periods at the start of the excitation periods, reflecting the switching loss.

Said discontinuity may be caused by a DC level shift in the excitation signal.

In a preferred embodiment, the excitation circuit of the communication device is provided with a controllable switching device serially arranged with the resonance circuit between first and second terminals of a voltage supply source and having a control terminal coupled to the input of the power amplifier for periodically supplying an excitation voltage signal to the resonance circuit, phase and/or frequency coupled with the modulated carrier signal circuit. In the excitation of the resonance circuit according to the invention, there is no necessity to minimize the switching signal transient time, i.e. to use an excitation signal with smooth signal transients. This allows to simplify the implementation of the communication device, in which said controllable switching device comprises a switch resistance serially arranged with the resonance circuit between the first and second terminals of said voltage supply source and being varied from a maximum resistance value to a minimum resistance value and vice versa to smoothen transients of said excitation voltage signal increasing above a threshold voltage within the excitation periods. In such communication device the controllable switching device may well comprise a MOS transistor having its drain source path serially coupled to the resonance circuit being controlled to vary the switch resistance stepwise.

In the communication device according to the invention the excitation of the resonance circuit not only tracks modulation dependent phase and/or frequency deviations of the modulated high frequency carrier input signal, but also allows to amplify modulation dependent envelope amplitude variations of said input signal, if any. The extra degree of freedom provided herewith makes it possible to comply with various different telecommunication standards, including those using constant envelope modulated high frequency carrier signals (such as e.g. GSM) and those using modulated envelope high frequency carrier signals (such as e.g. CDMA). When using an excitation circuit with a controllable switching device as indicated above, such communication device preferably comprises amplitude modulation means for modulating the amplitude of the supply voltage between the first and second terminals of the voltage supply source with modulation signal dependent envelope amplitude variations of the modulated high frequency carrier signal.

In allowing to use smooth signal transients, the invention enables to use bipolar transistor circuitry for the excitation of the resonance circuit. Another preferred embodiment of a communication device according to the invention is therefore characterized in that the excitation circuit comprises a charge pump supplying an excitation current signal, phase and/or frequency coupled with the modulated carrier signal circuit having smooth transients between a minimum and a maximum current level and increasing above a threshold current level within the excitation periods. In this embodiment, this threshold current level is chosen such that the part of the excitation current signal in excess of the threshold current level is determining and/or dominating the signal in the resonance circuit.

Such a communication device is preferably characterized in that an output stage of the charge pump comprises a bipolar transistor, the collector emitter path thereof being serially coupled to the resonance circuit between first and second terminals of a supply voltage source.

When using an excitation circuit with a charge pump as indicated above, a preferred embodiment of a communication device complying with telecommunication standards using modulated envelope high frequency carrier signals comprises amplitude modulation means for modulating the excitation signal as well as a supply voltage coupled to the resonance circuit with modulation signal dependent envelope amplitude variations of the modulated high frequency carrier signal.

Another preferred embodiment of a communication device is characterized in that the resonance circuit input means comprise a pulse generator controlling the excitation circuit to modulate the excitation signal in its phase and/or frequency and/or envelope amplitude in correspondence with the modulated high frequency carrier signal.

In telecommunication standards using constant envelope modulated high frequency carrier signals the envelope amplitude of the excitation signal is kept constant.

Another preferred embodiment of a communication device according to the invention is characterized by said antenna means having narrow bandwidth and being part of the resonance circuit.

This measure allows to combine main part of the resonance circuit functionality with the functionality of the antenna means, therewith providing an extensive integration of the resonance circuit with the antenna means and reducing the number of elements needed.

Preferably the antenna impedance is coupled to a tap of the inductor of said parallel LC circuit, which removes the need for an antenna impedance transformer.

The above and other object features and advantages of the present invention will be discussed more in detail hereinafter with reference to the disclosure of preferred embodiments and in particular with reference to the appended Figures, that show:

Figure 1 a blockdiagram of a communication device including a first embodiment of a power amplifier according to the invention;

Figure 2 a blockdiagram of a second embodiment of a power amplifier according to the invention;

Figures 3a,b signal plots showing the effect of an excitation signal having a 50% duty cycle on THD losses (curve C) when used in the power amplifier of Figure 1, in which the excitation circuit is provided with a MOS transistor output stage, the quality factor of the resonance circuit Q being 1.5 and the resonance frequency detuning rate being 60%;

Figures 4a,b signal plots showing the effect of an excitation signal having a 50% duty cycle on THD losses (curve C) and switching or excitation losses when used in the power amplifier of Figure 1, in which the excitation circuit is provided with a MOS

transistor output stage, the quality factor of the resonance circuit Q being 1.5 and the resonance frequency detuning rate being 27%;

Figures 5a,b signal plots showing the effect of an excitation signal having a 30% duty cycle on THD losses (curve C) and switching or excitation losses when used in the power amplifier of Figure 1, in which the excitation circuit is provided with a MOS transistor output stage, the quality factor of the resonance circuit Q being 3 and the resonance frequency detuning rate being 10%;

Figure 6 signal plots showing as a function of the inverse value of the quality factor of the resonance circuit which value of the excitation duty cycle and the detuning frequency results in a substantial elimination of respectively signal losses in the excitation circuit, THD losses and overall signal losses in the power amplifier as a whole.

Figure 7a-d various excitation signal forms usable in a communication device according to the invention;

Figure 8 a-c signal plots illustrating the functioning of the power amplifier according to the invention when being used to for amplifying an envelope amplitude modulated high frequency carrier signal

Figure 1 shows a blockdiagram of a communication device according to the invention, which is compliant to telecommunication standards using modulated envelope high frequency carrier signals (such as e.g. CDMA), including a power amplifier (1-5), preceded by a transmitter pre-stage unit 6 and followed by antenna means A. The transmitter pre-stage unit 6 is provided with an output supplying a high frequency carrier signal at a terminal Fc, a baseband modulation signal for modulating said high frequency carrier signal in phase and/or frequency at a terminal FM/PM, and a baseband modulation signal for modulating the envelope amplitude of said high frequency carrier signal at a terminal AM. With regard to the transmitter pre-stage unit 6 reference is made to existing prior art CDMA portable communication devices. Detailed knowledge of the transmitter pre-stage unit 6 is not needed to properly understand the invention, reason for which the unit 6 will not be further described.

The power amplifier (1-5) comprises a resonance circuit 1 arranged between resonance circuit input means 2 and the antenna means A, the resonance circuit input means 2 comprising an excitation circuit 3 coupled between a pulse generator 4 and the resonance circuit 1 for supplying an excitation signal thereto. The baseband modulation signals at the terminals PM/FM and AM, hereinafter referred to as PM/FM and AM baseband modulation signals respectively, and the high frequency carrier signal at the terminal Fc of the transmitter pre-stage unit 6 are supplied to the pulse generator 4, which derives therefrom control signal pulses for the excitation circuit 3. These pulses do not refer to a specific signal form, as will be explained hereinafter in more detail with reference to Figure 8 and may be rectangular, sinusoidal, Gaussian or otherwise.

The control signal pulses are generated at each period of the high frequency carrier signal phase and/or frequency modulated with the PM/FM baseband modulation signal with a duty cycle less than 50%. In addition thereto the pulse generator 4 also modulates the envelope amplitude of these control pulses with the AM baseband modulation signal. The circuitry needed to come to an excitation signal as defined hereabove, i.e. tracking the modulated high frequency carrier signal in its phase and/or frequency and/or amplitude and having a duty cycle less than 50%, can as such be designed and implemented by anyone skilled in the art to arrive at. In this connection, reference is made to Philips' pulse generator type PM 5786 B. The functionality of the pulse generator 4 may well be combined with the functionality of excitation circuit 3 in one single device.

The excitation circuit 3 comprises a charge pump with an output stage having a bipolar transistor, the collector emitter path thereof being serially coupled to the resonance circuit 1 between first and second terminals of a supply voltage source Vcc.

The resonance circuit 1 comprises a parallel RLC circuit directly coupled to the antenna means A. The resistor R represents mainly the radiation resistance of the antenna means A. The resonance frequency of the circuit 1 is chosen to correspond substantially to the carrier frequency (fcar) of the modulated high frequency carrier signal. The quality factor Q of the resonance circuit is preferably chosen to be greater than 1.

Furthermore, if the antenna means A are dimensioned to have a narrow bandwidth, then such narrow bandwidth antenna means can provide the functionality of the parallel RLC circuit to a great part. This removes the need to use a completely equipped RLC circuit in the resonance circuit 1, allowing to integrate the antenna means A as part of the power amplifier (1-5).

The pulse generator 4 controls the excitation circuit 3 to generate an excitation signal following the control pulses in their phase and/or frequency and their envelope amplitude modulation, and having continuous transients between a minimum and a maximum current level, the excitation current signal exceeding 50% of the maximum current level during a periodic time interval smaller than 50% of the repetition time of the input signal. The excitation signal excitates the resonance circuit 1, therewith bringing this circuit in a resonance mode in accordance with the invention.

In addition thereto the supply voltage Vcc is amplitude modulated with the AM baseband modulation signal through an amplitude modulator 5, which is coupled to the terminal AM of the transmitter pre-stage unit 6. With regard to this amplitude modulator 5, reference is made to Philips' IC LM 78xx or equivalent ICs.

The functioning of the power amplifier with regard to AM modulations will be explained with reference to Figures 8a-c.

Figure 2 shows a blockdiagram of a second embodiment of a power amplifier for use in a communication device according to the invention in which elements corresponding to those of Figure 1 have the same references. The excitation circuit 3 now comprises a switching device using a MOS transistor having its drain source path serially arranged with the resonance circuit 1 between first and second terminals of a supply voltage source, respectively connected to mass and a supply voltage Vcc. For AC signals both first and second terminals may be considered to be massconnected.

In the resonance circuit 1 the capacitor C is parallel connected to the inductor L, but unlike the resonance circuit of Figure 1, the inductor L is now provided with first and second taps, T1 respectively T2. The first tap T1 is coupled to the resistor R and the second supply voltage terminal, the second tap T2 is coupled to the output of the excitation circuit 3, therewith therewith providing proper antenna impedance matching without using an extra impedance transformer.

Figures 3a-c show signal plots illustrating the effect of an excitation signal (curve A) having a 50% duty cycle on THD losses (curve C) when used in the power amplifier of Figure 1, in which the excitation circuit is provided with a MOS transistor output stage, the quality factor of the resonance circuit Q being 1.5 and the resonance frequency detuning rate (dfres) being 60%. The switching losses are practically zero. The THD losses being derived from the difference

between the first order harmonic frequency of the resonance circuit uotput signal indicated by curve B and the curve A excitation signal are considerable and may be used as a reference for the THD losses occurring in the cited prior art power amplifier.

Figures 4a-c show signal plots illustrating the effect of an excitation signal having a 50% duty cycle (curve A) on THD losses (curve C) and switching or excitation losses when used in the power amplifier of Figure 1, in which the excitation circuit is provided with a MOS transistor output stage, the quality factor of the resonance circuit Q being 1.5 and the resonance frequency detuning rate being 27%. Now switching losses are appearing, reflected in a discontinuity at point D of curve A, however, the reduction in THD losses is much greater than these switching losses, as is shown in curve C. The net reduction effect of detuning of the resonance frequency of the resonance circuit on the overall power loss is demonstrated herein to improve the efficiency of the above cited power amplifier, i.e. also with an excitation duty cycle of 0.5.

Figures 5a-c show signal plots illustrating the effect of an excitation signal (curve A) having a 30% duty cycle on THD losses (curve C) and switching or excitation losses when used in the power amplifier of Figure 1, in which the excitation circuit is provided with a MOS transistor output stage, the quality factor of the resonance circuit Q being 3 and the resonance frequency detuning rate being 10%. Here, an optimal trade off between switching and THD losses is obtained, resulting in a minimised overall power loss of the power amplifier.

Figure 6 shows the interrelationship between the three parameters: excitation duty cycle (Tex/Tcar), the resonance frequency detuning rate (dfres) and quality factor (Q) of the resonance circuit in signal plots indicating as a function of the inverse value of the quality factor (1/Q) of the resonance circuit respectively in curve A which value of the resonance frequency detuning rate (dfres), in curve B which value of the excitation duty cycle when approximated by (1/Q), in curve C which value of the excitation duty cycle and in curve D which value of the resonance frequency detuning rate (dfres) when approximated by $(4/Pi)(1/Q)^2$ results in a substantial elimination of respectively signal losses in the excitation circuit. The curves A and C are based respectively on the following formulas:

$$\mathrm{dfres}[Q] = \frac{\mathrm{Sqrt}\left[1 - \left(1 - \frac{1}{Q}\right)^4\right]}{2\,\mathrm{Pi}\left(1 - \frac{1}{Q}\right)^2} + \frac{3 + \frac{2\,\mathrm{ArcSin}\left[\left(1 - \frac{1}{Q}\right)^2\right]}{\mathrm{Pi}}}{4} - 1$$

$$(\mathrm{Tex}/\mathrm{Tcar})[Q] = \frac{\mathrm{Sqrt}\left[1 - \left(1 - \frac{1}{Q}\right)^4\right]}{2\,\mathrm{Pi}\left(1 - \frac{1}{Q}\right)^2 \left(\frac{\mathrm{Sqrt}\left[1 - \left(1 - \frac{1}{Q}\right)^4\right]}{2\,\mathrm{Pi}\left(1 - \frac{1}{Q}\right)^2} + \frac{3 + \frac{2\,\mathrm{ArcSin}\left[\left(1 - \frac{1}{Q}\right)^2\right]}{\mathrm{Pi}}}{4}\right)}$$

THD losses are minimised for zero value of the excitation duty cycle (Tex/Tcar) and the resonance frequency detuning rate (fres/fcar-1), which correspond to the horizontal X coordinate.

Curve E shows a trade off between switching and THD losses according to the invention, which is based on taking 50% of the value for the resonance frequency detuning rate necessary to minimise switching losses. This value results in an overall reduction of power loss in the power amplifier as a whole and is most likely to lead to the most optimal trade off. However, in practise, it may well be that a value somewhat deviating from the abovementioned value of 50% for the resonance frequency detuning rate (dfres) will give a somewhat better trade off in terms of minimum overall power loss.

The signal plot clearly shows that substantial elimination of signal losses in the excitation circuit does not depend on the duty cycle. Even for duty cycles greater than 0.5 relative to the carrier signal period these excitation losses can be eliminated.

A commercially interesting optimization area is defined by values of the duty cycle between approximately 0.1 and 0.5 relative to the carrier signal period. The following table is to demonstrate the effect of the optimal trade off between switching or excitation losses and THD losses according to the invention on the reduction in the overall signal losses in quantitive form.

		(Tex/Tcar)=0.5 dfres chosen to minimise switching losses		Optimal trade off between THD losses & switching losses		Dfres=0 (fres=fcar) Minimum THD losses	
Duty cycle (Tex/Tcar)	Q	Dfres	efficiency	Dfres	Efficiency	Dfres	Efficiency
0.5	1.75	0.6	69 %	0.3	84 %	0	69 %
0.4	2.13	0.34	84 %	0.17	91 %	0	81 %
0.3	2.8	0.16	92 %	0.08	95 %	0	88 %
0.2	4.35	0.07	95 %	0.035	96 %	0	91 %

It will be clear, that the invention is not limited to a 50% value for the resonance frequency detuning rate to come to an effective trade off between excitation loss and THD loss leading to a overall reduction of the power loss of the power amplifier as a whole. Values for the resonance frequency detuning rate resulting in such effective trade off may vary within an order of magnitude of 50%. Furthermore, dependent on the specific application of the power amplifier, it may well be that excitation losses are to be suppressed to larger extend than THD losses, or vice versa. The resonance frequency detuning rate can be chosen to meet the requirements of said specific application.

The curves also show that an increasing the quality factor of the resonance circuit (Q) allows to decrease the resonance frequency detuning rate dfres as well as the excitation duty cycle (Tres/Tcar) to arrive at an optimal trade off in terms of minimised overall power loss. Dependent on this Q factor the excitation duty cycle may be chosen below the abovementioned value of the

order of magnitude of 0.1, and the resonance frequency detuning rate dfres may be chosen close to the carrier frequency (fcar) of the high frequency carrier signal.

Figures 7a-d show four various excitation signal forms a-d usable in a communication device according to the invention. These signals all have a duty cycle less than 50% and continuous transients between a minimum and a maximum level, the signal exceeding 50% of the maximum current level during a periodic time interval smaller than 50% of its repetition time.

Figure 8 a-c show signal plots illustrating the functioning of the power amplifier according to the invention when being used for amplifying an envelope amplitude modulated high frequency carrier signal with a digital AM baseband modulation signal as depicted in Figure 8b.

Figure 8a shows the result of AM modulation of an otherwise unmodulated (i.e. without PM and/or FM modulations) high frequency carrier signal obtained with the communication device of Figure 1. In order to allow the resonance signal amplitude to vary with the AM modulation signal both excitation signal and supply voltage have to be amplitude modulated. The minimum voltage level occurring at the resonance circuit remains constant as shown in Figure 8a, whereas the transmitted antenna signal is varying symmetrically around zero level as is shown in Figure 8c.

When using the power amplifier of Figure 2, the excitation doesn't need to be varied and variation of the supply voltage with the AM baseband modulation signal suffices. This results again in a signals as shown in Figures 8a and 8c.

The possibility to arrive at a high frequency carrier transmitter signal being PM and/or FM modulated as well as AM modulated allows to use the communication devices according to the invention in telecommunication standard, such as e.g. CDMA. However, by keeping the envelope of the a high frequency carrier transmitter signal constant these communication devices may also be used in telecommunication standard such as e.g. GSM.

In a prototype power amplifier as shown in Figure 1 using a charge pump in the excitation circuit 3, the following relationships between the quality of the resonance circuit 1 and the duty cycle of the excitation signal used, were measured:

	Q = 2	4	6	8	10
duty cycle = 50%	68	67	66	65	64
45 %	74	74	73	72	71
32 %	85	88	88	88	86
25 %	83	91	92	92	90
14 %	70	85	91	93	93
4 %	63	76	83	87	88

Significant improvements in efficiency are obtained within the area defined by a quality factor greater than an order of magnitude of 2 and a duty cycle of the excitation signal less than an order of magnitude of 40%.

In the above the invention is explained with a voltage and current like excitation of the resonance circuit, bounding the area of characteristics of circuitry, which can be used to materialize the invention. It is clear that the invention may well be applied with any implementation of the excitation circuit 3 having a mixed current/voltage output characteristic.

Furthermore the signal forms usable for an excitation in accordance with the invention are not limited to the ones shown in Figures 7a-d and include any form within the definition given in the claims.

The invention removes the necessity to use a bandpassfilter, however, such use is not precluded.

Claims:

1 A communication device including a power amplifier for amplifying a modulated high frequency carrier input signal comprising a resonance circuit and an excitation circuit for a signal excitation in the resonance circuit phase and/or frequency coupled with the modulated high frequency carrier signal, characterized by said excitation occurring within excitation periods (Tex) in a periodic alternation with resonation periods (Tfre), during which the resonance circuit is in a free running resonance mode, the excitation periods being smaller than the resonation periods to define an excitation duty cycle (Tex/Tcar) relative to the period of the carrier signal (Tcar) of less than 0.5.

2 A communication device according to claims 1, characterized by the resonance circuit having a resonance frequency (fres) higher than the carrier frequency (fcar) of the modulated high frequency carrier signal over a resonance frequency detuning rate (dfres), defined by the frequency deviation of said resonance frequency from said carrier frequency relative to the carrier frequency (fres/fcar-1), substantially at most corresponding to half the excitation duty cycle.

3 A communication device according to claim 1 or 2, characterized by said resonance frequency detuning rate (dfres) being in the order of magnitude of the half square value of said excitation duty cycle (Tex/Tcar) for an excitation duty cycle above an order of magnitude of 0.1.

4 A communication device according to one of claims 1 to 3, characterized by the excitation duty cycle (Tex/Tcar) being defined to decrease with increasing quality factor (Q) of the resonance circuit and vice versa for an excitation duty cycle (Tex/Tcar) above an order of magnitude of 0.1.

5 A communication device according to one of claims 1 to 4, characterized by an excitation duty cycle (Tex/Tcar) and a resonance frequency detuning rate (dfres=fres/fcar–1) being substantially defined by:

$$(Tex/Tcar)[Q] = \frac{\mathrm{Sqrt}\left[1-\left(1-\frac{1}{Q}\right)^4\right]}{2\,\mathrm{Pi}\left(1-\frac{1}{Q}\right)^2\left(\frac{\mathrm{Sqrt}\left[1-\left(1-\frac{1}{Q}\right)^4\right]}{2\,\mathrm{Pi}\left(1-\frac{1}{Q}\right)^2}+\frac{3+\frac{2\,\mathrm{ArcSin}\left[\left(1-\frac{1}{Q}\right)^2\right]}{\mathrm{Pi}}}{4}\right)}$$

6. A communication device according to one of claims 1 to 5, characterised by a resonance frequency detuning rate (dfres=fres/fcar-1) being substantially defined by:

$$dfres[Q]=0.5\left[\frac{\mathrm{Sqrt}\left[1-\left(1-\frac{1}{Q}\right)^4\right]}{2\,\mathrm{Pi}\left(1-\frac{1}{Q}\right)^2}+\frac{3+\frac{2\,\mathrm{ArcSin}\left[\left(1-\frac{1}{Q}\right)^2\right]}{\mathrm{Pi}}}{4}-1\right]$$

7. A communication device according to one of claims 1 to 6, characterized by a discontinuity in the slope of the signal occurring in the resonance circuit during the resonation periods at the start of the excitation periods.

8. A communication device according to claim 7, characterized by a DC level shift causing said discontinuity to occur.

9. A communication device according to one of claims 1 to 8, characterized in that the excitation circuit comprises a controllable switching device serially arranged with the resonance circuit between first and second terminals of a voltage supply source and having a control terminal coupled to the input of the power amplifier for periodically supplying an excitation voltage signal to the resonance circuit, phase and/or frequency coupled with the modulated carrier signal circuit.

10. A communication device according to claim 9, characterized in that the controllable switching device comprises a switch resistance serially arranged with the resonance circuit between the first and second terminals of said voltage supply source and being varied from a maximum resistance value to a minimum resistance value and vice versa to smoothen transients of said excitation voltage signal increasing above a threshold voltage within the excitation periods.

11. A communication device according to claim 10, characterized in that the controllable switching device comprises a MOS transistor having its drain source path serially coupled to the resonance circuit being controlled to vary the switch resistance stepwise.

12. A communication device according to one of claims 9 to 11, characterized by amplitude modulation means for modulating the amplitude of the supply voltage between the first and second terminals of the voltage supply source with modulation signal dependent envelope amplitude variations of the modulated high frequency carrier signal.

13. A communication device according to one of claims 1 to 8, characterized in that the excitation circuit comprises a charge pump supplying an excitation current signal, phase and/or frequency coupled with the modulated carrier signal circuit having smooth transients between a minimum and a maximum current level and incraesing above a threshold curent level within the excitation periods.

14. A communication device according to claim 13, characterized in that an output stage of the charge pump comprises a bipolar transistor, the collector emitter path thereof being serially coupled to the resonance circuit between first and second terminals of a supply voltage source.

15. A communication device according to claim 13 or 14, characterized by amplitude modulation means for modulating the excitation signal as well as a supply voltage coupled to the resonance circuit with modulation signal dependent envelope amplitude variations of the modulated high frequency carrier signal.

16. A communication device according to one of claims 1 to 15, characterized in that the resonance circuit input means comprise a pulse generator controlling the excitation circuit to modulate the excitation signal in its phase and/or frequency and/or envelope amplitude in correspondence with the modulated high frequency carrier signal.

17. A communication device according to one of claims 1 to 16, characterized by the resonance circuit having a resonance filter quality factor greater than 1.

18. A communication device according to one of claims 1 to 17, characterized by a balanced implementation of the excitation circuit and the resonance circuit.

19. A communication device according to one of claims 1 to 18, characterized in that the resonance circuit comprises a parallel RLC network, an inductor and resistor thereof being part of the antenna means.

20. A communication device according to one of claims 1 to 19, characterized in that the resonance circuit comprises a parallel RLC circuit comprising an inductor provided with a tapped coupling to the antenna impedance.

21. A communication device according to claim 20, characterized in that the inductor is provided with a further tap, coupled to the excitation circuit.

22. A communication device according to one of claims 1 to 21, characterized by said antenna means having narrow bandwidth.

23. High frequency power amplifier for use in a communication device according to one of claims 1 to 19, characterized by a resonance circuit part provided with antenna coupling means for completing the resonance circuit part to form said resonance circuit by coupling antenna means thereto.

86

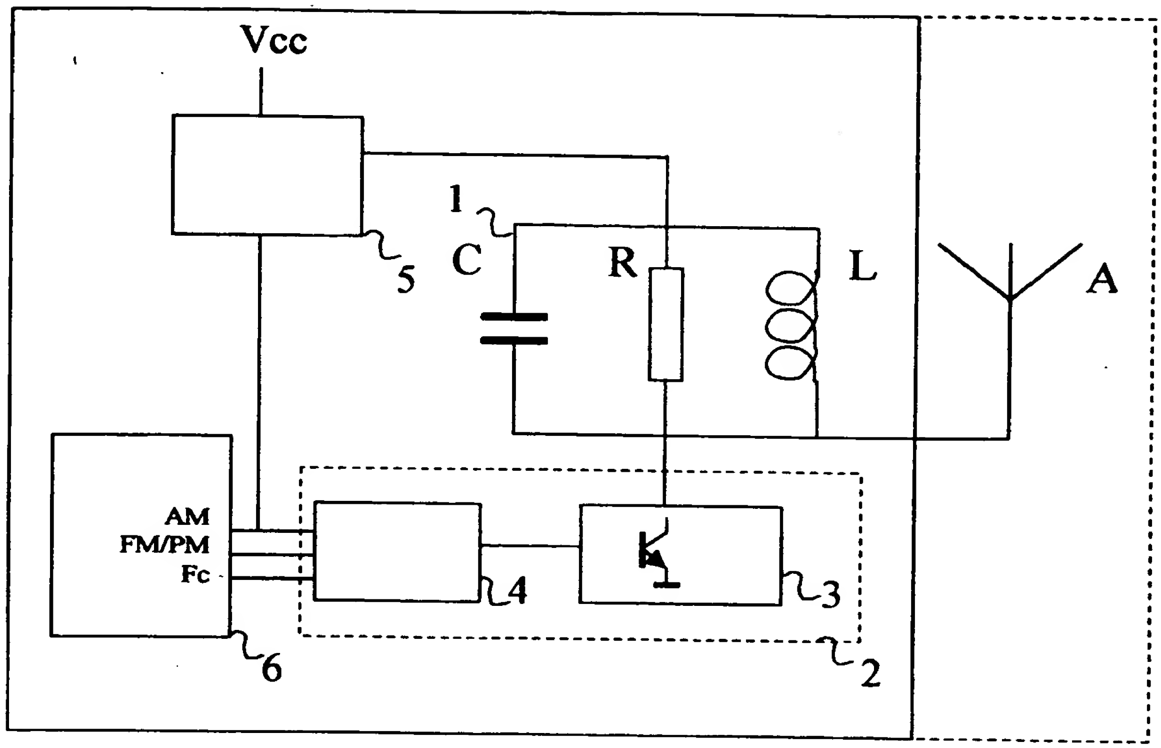


Fig. 1

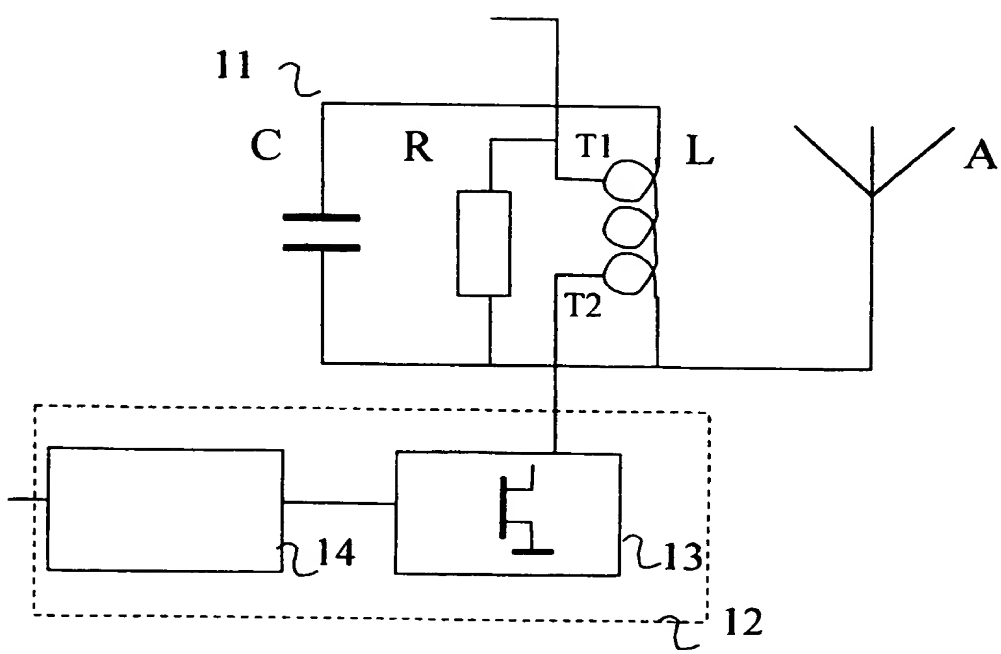


Fig. 2

PA CLAM2 CIR Temperature = 27

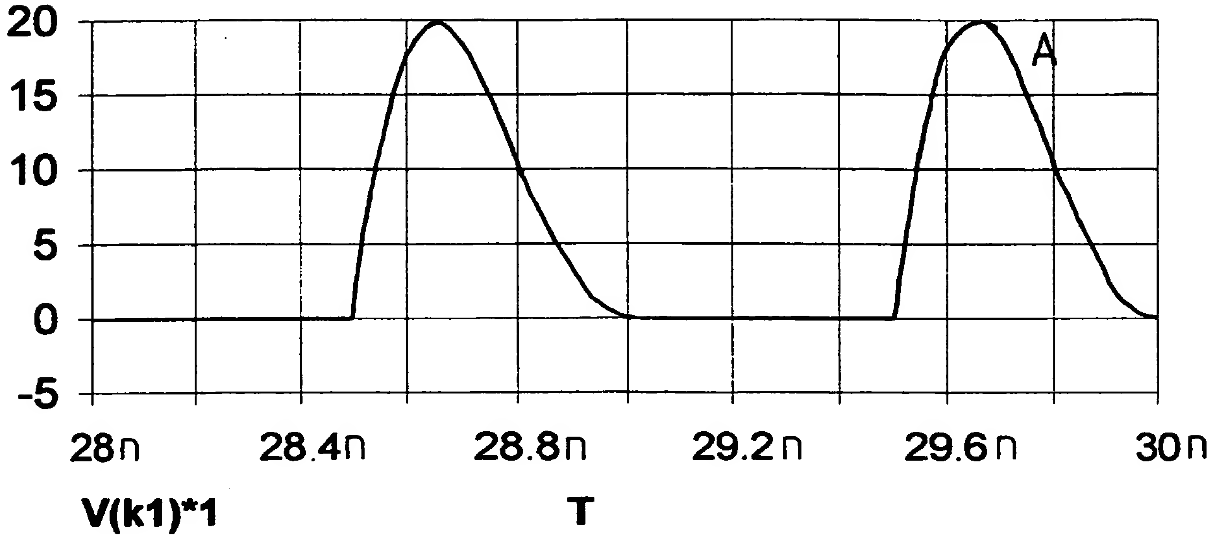


Fig. 3a

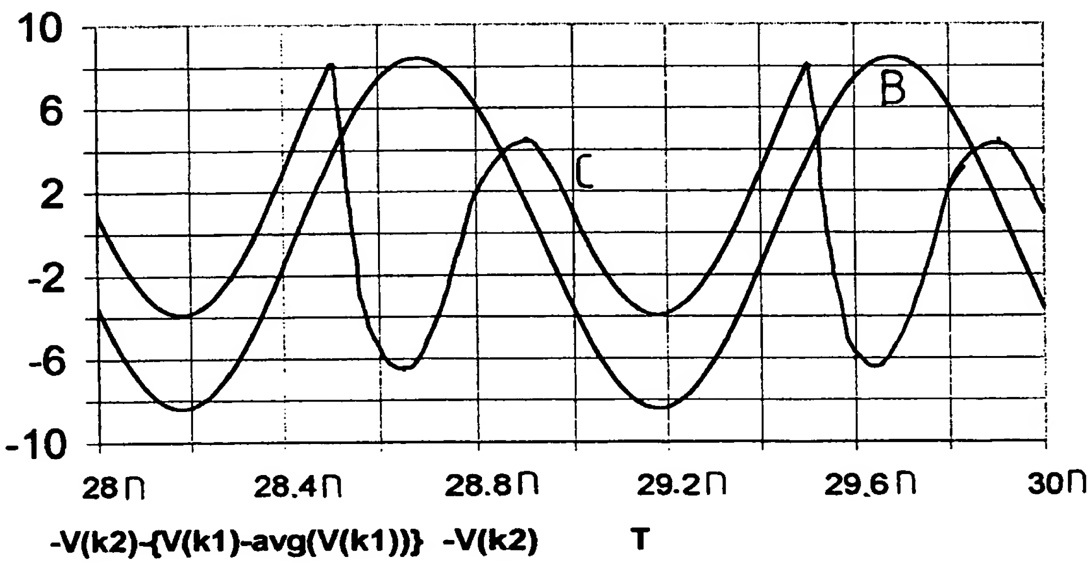


Fig. 3b

PA CLAM2 CIR Temperature = 27

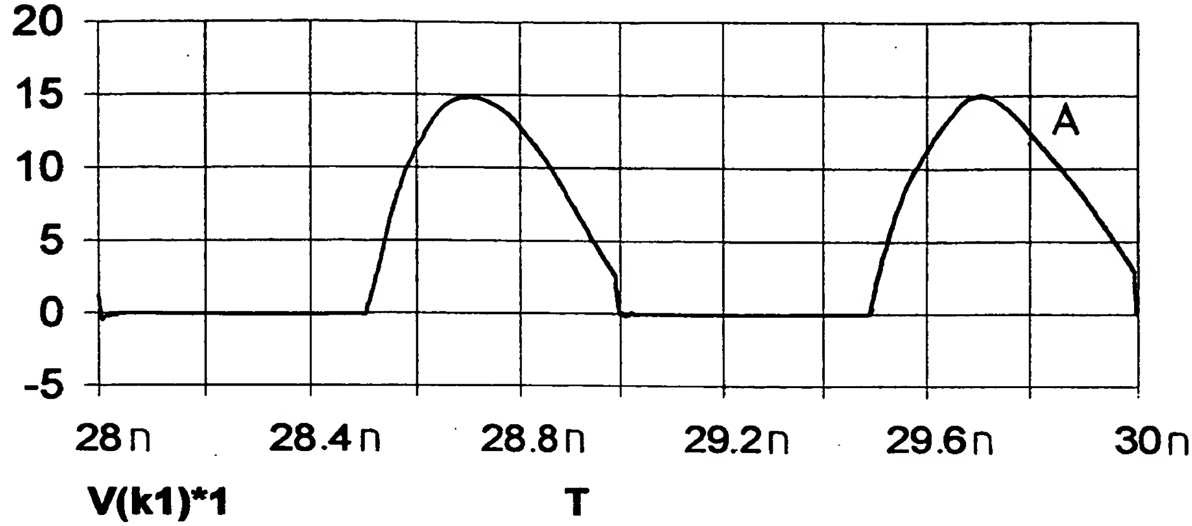


Fig. 4a

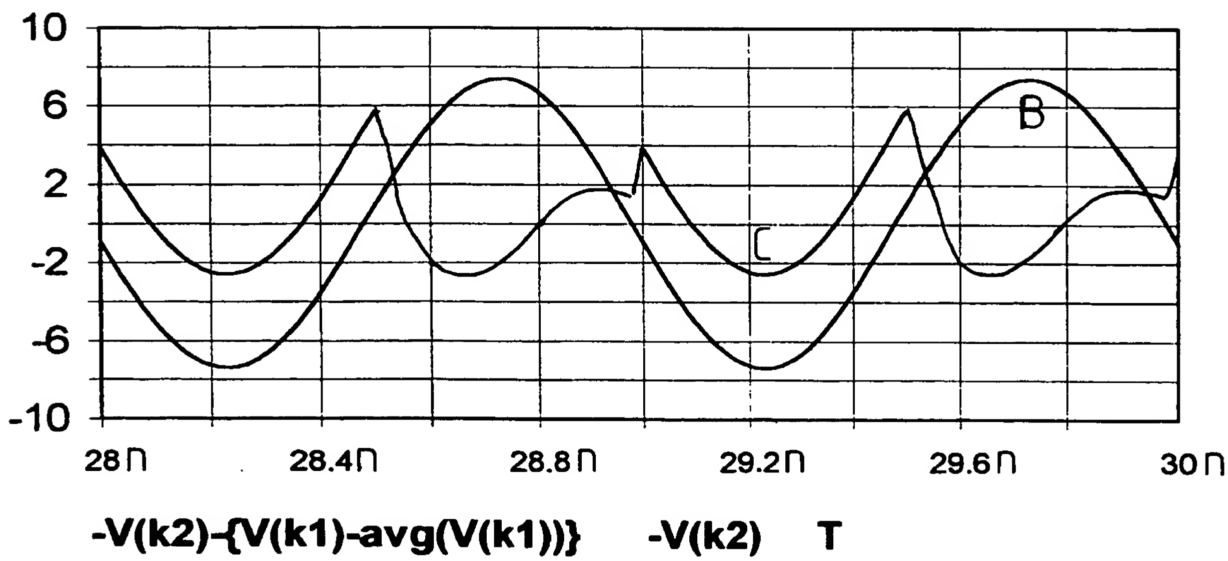


Fig 4b

PA CLAM2 CIR Temperature = 27

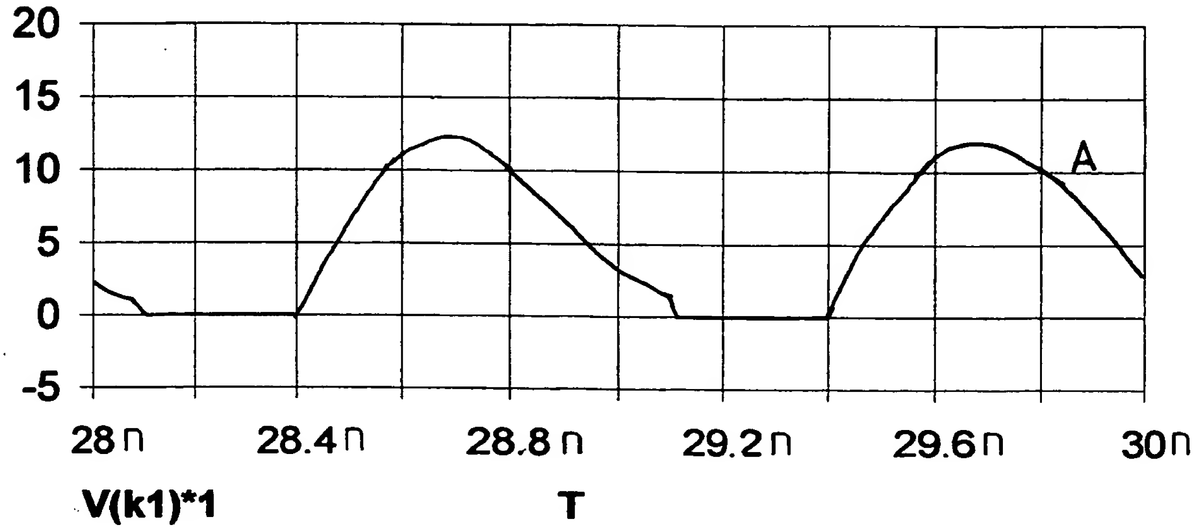


Fig. 5a

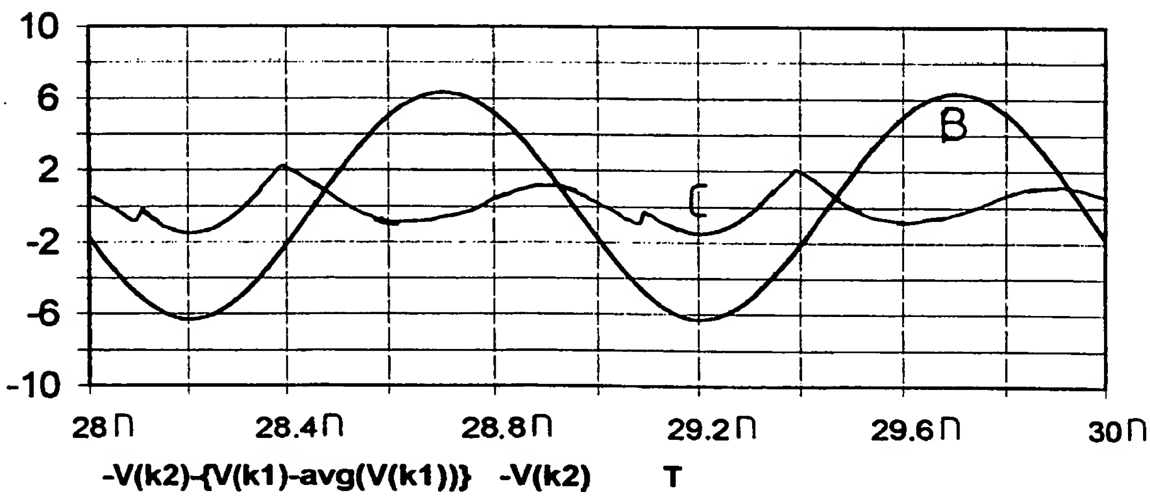


Fig 5b

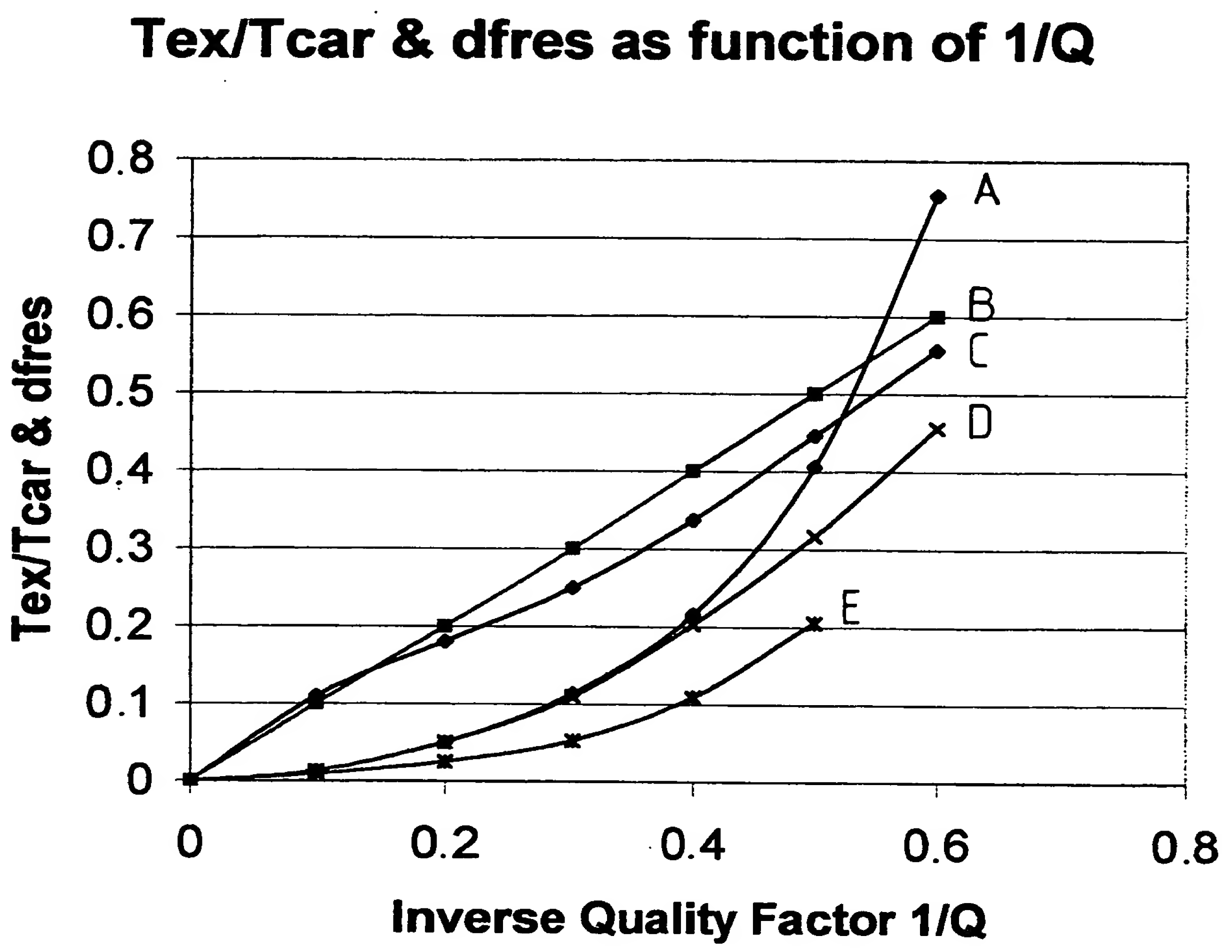

Tex/Tcar & dfres as function of 1/Q
Tex/Tcar & dfres
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
A
B
C
D
E
0
0.2
0.4
0.6
0.8
Inverse Quality Factor 1/Q

Fig. 6

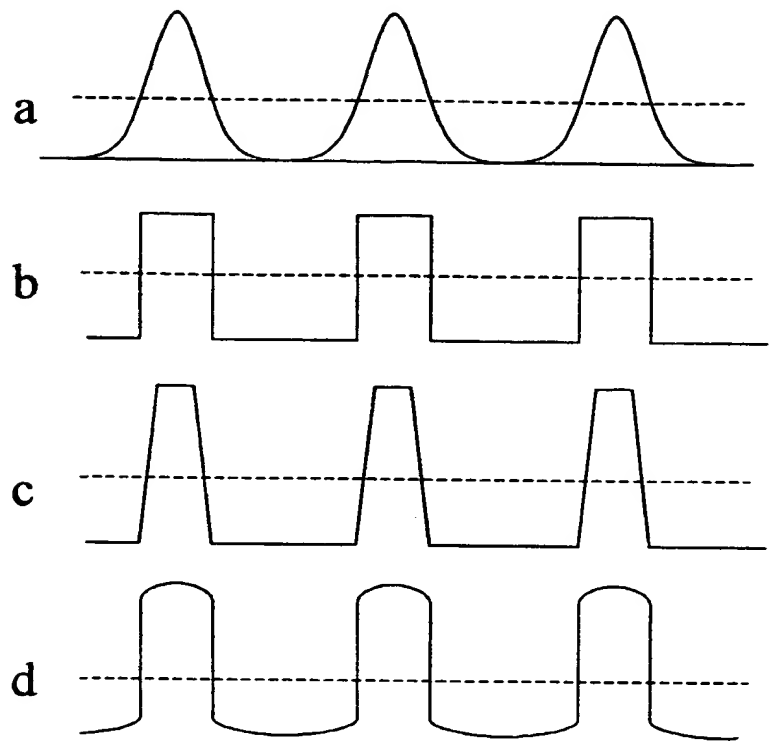


Fig 7

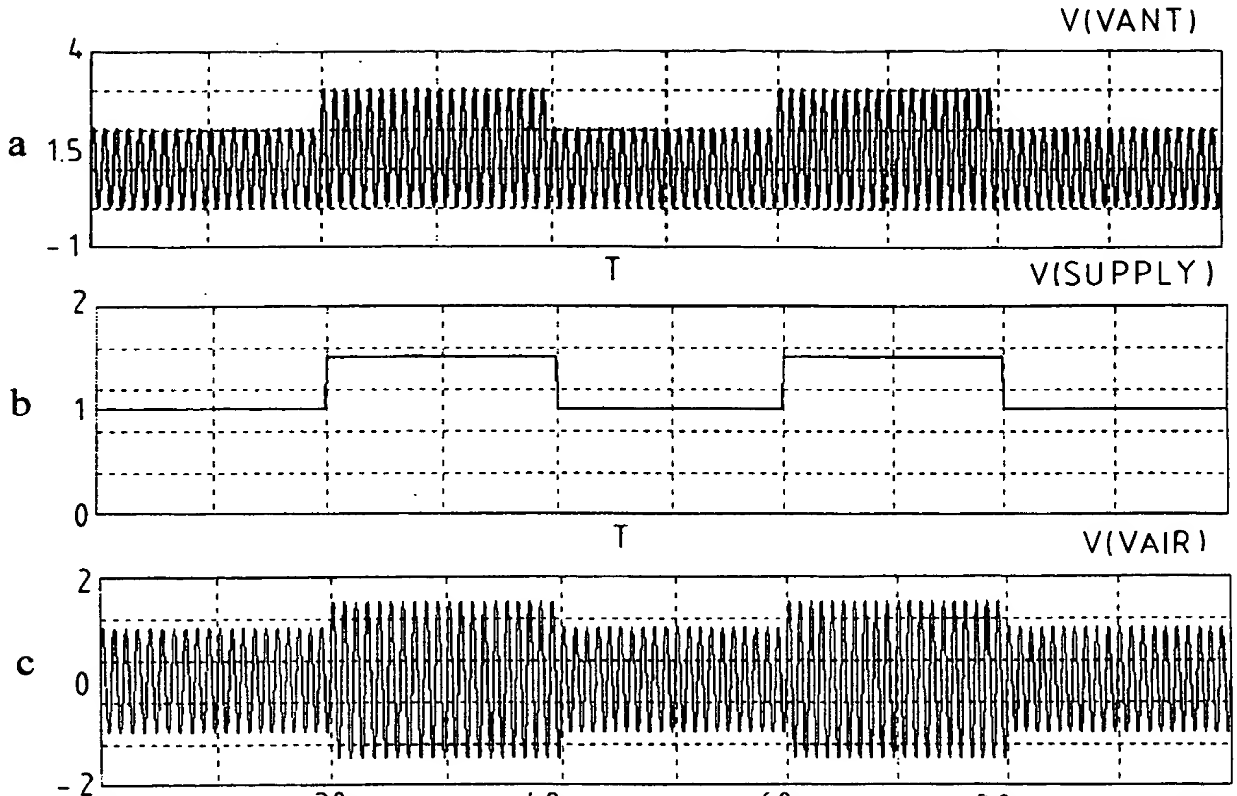

V(VANT)
a
4
1.5
-1
T
V(SUPPLY)
b
2
1
0
T
V(VAIR)
c
2
0
-2
0n
20n
40n
60n
80n
100n

Fig 8

INTERNATIONAL SEARCH REPORT

International Application No
PCT/EP 00/03203

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03F3/217 H04B1/04

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03F H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 717 884 A (MITZLAFF JAMES E) 5 January 1988 (1988-01-05) column 2, line 53 -column 3, line 60; figures 1-4	1
A	US 3 648 188 A (RATCLIFF HENRY K) 7 March 1972 (1972-03-07) column 2, line 10 -column 5, line 25; figures 1-4	1-6, 9-11,13, 17,19,23

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
31 July 2000	04/08/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Andersen, J.G.

1

Form PCT/ISA/210 (second sheet) (July 1992)

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	JOCHEN P: "KLASSE-E-VERSTAERKER MIT MAXIMALER AUSGANGSLEISTUNG" FREQUENZ, vol. 44, no. 9 / 10, 1 September 1990 (1990-09-01), pages 262-266, XP000165295 ISSN: 0016-1136 paragraphs ‘0003!,‘0004!,‘0006!; figures 1,6 ---	1-23
A	TIRDAD SOWLATI ET AL: "LOW VOLTAGE, HIGH EFFICIENCY CLASS E GAAS POWER AMPLIFIERS FOR MOBILE COMMUNICATIONS" TECHNICAL DIGEST OF THE GALLIUM ARSENIDE INTEGRATED CIRCUIT SYMPOSI (GAAS IC), PHILADELPHIA, OCT. 16 - 19, 1994, no. SYMP. 16, 16 October 1994 (1994-10-16), pages 171-174, XP000482733 INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS ISBN: 0-7803-1976-1 the whole document -----	1-23

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/EP 00/03203

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 4717884 A	05-01-1988	NONE	
US 3648188 A	07-03-1972	CA 939759 A	08-01-1974
		DE 2126469 A	22-06-1972
		FR 2096158 A	11-02-1972
		GB 1290304 A	27-09-1972
		NL 7107952 A	14-12-1971
		SE 376133 B	05-05-1975